Electrical Properties of Metal-Ferroelectric-Insulator-Semiconductor Field-Effect Transistor Using an Au/$(Bi,La)_4Ti_3O_{12}$/$LaZrO_x$/Si Structure

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Abstract: We fabricated the metal-ferroelectric-insulator-semiconductor filed-effect transistors (MFIS-FETs) using the $(Bi,La)_4Ti_3O_{12}$ and $LaZrO_x$ thin films. The $LaZrO_x$ thin film had a equivalent oxide thickness (EOT) value of 8.7 nm. From the capacitance-voltage (C-V) measurements for an Au/$(Bi,La)_4Ti_3O_{12}$/$LaZrO_x$/Si MFIS capacitor, a hysteric shift with a clockwise direction was observed and the memory window width was about 1.4 V for the bias voltage sweeping of ±9 V. From drain current-gate voltage (I_D-V_G) characteristics of the fabricated Fe-FETs, the obtained threshold voltage shift (memory window) was about 1 V due to ferroelectric nature of BLT film. The drain current-drain voltage (I_D-V_D) characteristics of the fabricated Fe-FETs showed typical n-channel FETs current-voltage characteristics.

Key Words : ferroelectrics, memory, MFIS, FET, $(Bi,La)_4Ta_3O_{12}$, $LaZrO_x$

1. Introduction

One-transistor type ferroelectric-gate field-effect transistors (Fe-FETs) have attracted much attention, because of their potential such as low-power consumption, non-destructive read-out operation, and high density integration [1]. Some recent reports about the Fe-FETs with a gate stack of metal-ferroelectric-insulator-semiconductor (MFIS) show the advance in device operation properties [2].

In an MFIS gate stack, high dielectric constant of a buffer insulator is desirable for the effective distribution of a bias voltage to the ferroelectric film [3,4]. Among the available high-k dielectrics, $LaZrO_x$ is attractive as a buffer insulator for its high dielectric constant (~20) and high crystallization temperature [5]. Additionally, we chose the $(Bi,La)_4Ti_3O_{12}$ (BLT) film as a ferroelectric layer. The BLT film had been suggested as the most suitable ferroelectric material for the Fe-FETs so far, because of its fatigue-free and long-retention properties, and low processing temperature [6].

In this study, we fabricated the MFIS-FETs using the BLT and $LaZrO_x$ thin films. Then we characterized the electrical properties of the MFIS gate stack and the MFIS-FETs.

2. Experiments

To fabricate an MFIS capacitor, we deposited the BLT and $LaZrO_x$ thin films on the Si substrate using a sol-gel spin-coating method. The phosphorus-diffused source- and drain-region were first formed on the Si substrate. The $LaZrO_x$ solution was spun-coated on Si, dried at 400 ℃ and finally annealed at 750 ℃. Then the BLT films were spun-coated on the $LaZrO_x$/Si structure. The stoichiometric composition of the BLT solution was Bi:La:Ti=3.25:0.75:3. After BLT films were repetitively coated and dried to obtain the desired thickness, films were finally crystallized at 750 ℃ for 30 minutes. The typical thickness of the BLT and $LaZrO_x$ thin films were about 420 nm and 30 nm, respectively. The contact holes were opened on the source- and drain-region by wet chemical etching with the HCl and buffered HF mixture. Au thin film was thermally evaporated on the surface as a gate metal and contact pads.

The electrical properties of the MFIS-FETs and its gate stack, Au/BLT/$LaZrO_x$/Si MFIS capacitor, were characterized. The capacitance-voltage (C-V) measurement was carried out with the HP-4280A. Drain current-drain voltage (I_D-V_D) and drain current-gate voltage (I_D-V_G) characteristics were measured using the HP-4156C.

3. Results and Discussion

First, we investigated the C-V characteristics of an Au/$LaZrO_x$/Si metal-insulator-semiconductor (MIS) capacitor. Figure 1 shows a high-frequency C-V characteristic curve measured with the bias voltage sweeping of ±5 V. We observed the negligibly small hysteresis in the curve, which implied the charge injection or mobile ions were negligible. From the accumulation capacitance value, the equivalent oxide thickness (EOT) value was determined as about 8.7 nm. In order to distribute the bias voltage enough to the ferroelectric layer, a buffer insulator in an MFIS-FETs should have a small EOT. However, the $LaZrO_x$ thin film, in this study, had a relatively large EOT value which might be due to the low-k oxide layer formed at the interface during annealing processing.

The C-V characteristic curves with a different voltage sweeping for the Au/BLT/$LaZrO_x$/Si stack are illustrated in Fig. 2(a). The C-V curve exhibited a clockwise hystersis loop attributed to the ferroelectric behavior of the BLT film. The memory window width, calculated from the shift of the flat band voltage, increased as the applied voltage increased. These results were considered to

be due to the fact that the BLT film has a good ferroelectric property. Figure 2(b) summarizes the relationship between the bias voltage sweeping and the memory window width. The value of the memory window width gradually increased up to 1.4 V as the bias voltage sweeping increased to ±9 V. For the more larger bias voltage, however, the memory window width did not increase, but rather decreased. It might be considered to be due to the charge injection effects.

Figure 3(a) shows the I_D-V_G curve of the Fe-FETs using an Au/BLT/$LaZrO_x$/Si gate stack. A hysteresis loop with a counter-clockwise direction was observed as it was indicated by arrows in the figure. During the measurement, the gate voltage was swept forward and backward in the range of ±5 V, while the drain voltage was fixed at 0.1 V. It was also found that the leakage current density was as low as $1.5x10^{-7}$ A. The obtained threshold voltage shift (memory window width) was about 1 V. The I_D-V_D curve of the Fe-FETs shown in Fig. 3(b), exhibits typical current-voltage characteristics of an n-channel field-effect transistor. The saturated drain current at a gate voltage of 4 V was about three orders of magnitude larger than that for 0 V.

4. Conclusions

We fabricated the MFIS-FETs using the BLT and $LaZrO_x$ thin films. The $LaZrO_x$ thin film deposited on Si, showed a good electrical property. The C-V measurement revealed that the Au/BLT/$LaZrO_x$/Si MFIS capacitor had good ferroelectric properties. The memory window width was as large as 1.4 V for the bias voltage sweeping of ±9 V. From the I_D-V_G and I_D-V_D characterization, the MFIS-FETs showed typical n-channel FETs current-voltage characteristics with a memory window width of 1 V.

Acknowledgement

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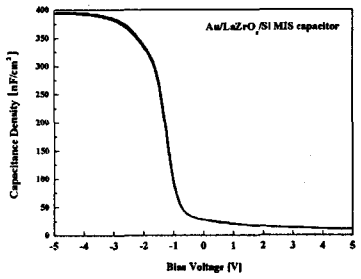

Figure. 1. C-V characteristics of the Au/$LaZrO_x$/Si capacitor.

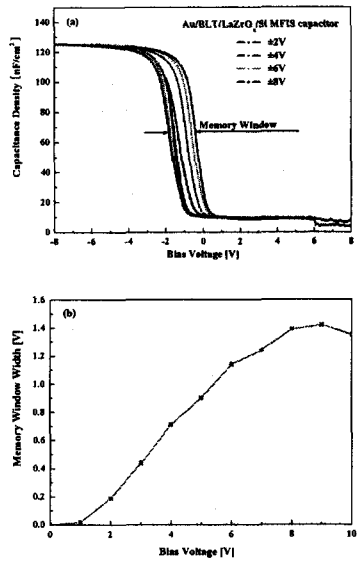

Figure 2. (a) C-V characteristic curves of the Au/BLT/$LaZrO_x$/Si capacitor and (b) variation of memory window width according to the bias voltage sweeping.

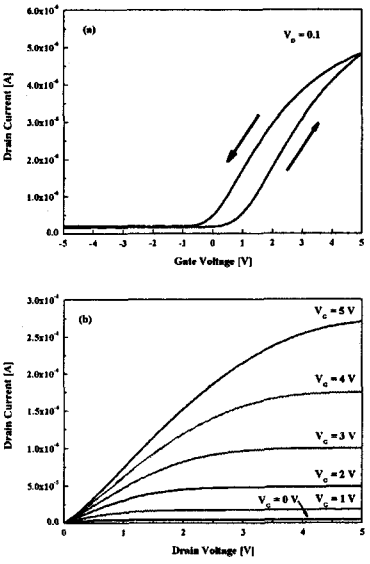

Figure 3. (a) I_D-V_G and (b) I_D-V_D characteristic curves for the n-channel MFIS-FET with the Au/BLT/$LaZrO_x$/Si gate stack.