BA03

Spin-transfer Torque RAM (STT-RAM) Technology

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Spin-transfer torque writing technology[1], combined with the newly-observed high tunnelling magnetoresistance (>300%) in MgO magnetic tunnel junctions (MTJs)[2], provides an exciting path to realize Gbit-scale STT-RAM (Spin-Transfer Torque RAM) with low power consumption, fast operation speed (few ns), and excellent scalability to future semiconductor nodes. The intrinsic attributes of STT-RAM are attractive for replacing not only existing non-volatile memory products, but also Random Access Memory (RAM), such as SRAM and DRAM, in wireless and embedded applications. We have previously reported on spin-transfer torque switching (STS) in MgO tunnel junctions[3]. I will first describe the physics and mechanisms underlying STS and our recent experimental results showing spin-transfer switching in MgO MTJ bit-cells and how these results relate to our micro-magnetic and theoretical models of switching. The techniques involved in reducing the critical STS current and achieving consistent switching in the nanosecond regime will be presented and discussed, along with most recent integrated circuit results. I will also highlight the key advantages of spin-transfer torque writing technology and the technical issues in commercializing STT-RAM. Finally, the potential applications of STT-RAM in mobile devices, digital consumer electronics and automotive products will be outlined.

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BA04

2Mb SPRAM Design: Bi-Directional Current Write and Paralelizing-Direction Current Read Schemes Based on Spin-Transfer Torque Switching

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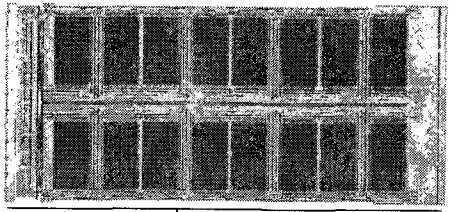
Magnetic tunnel junction with MgO tunneling barrier offers TMR ratio over 100% (up to 472% [1])and reduced threshold current (write current) density under 500uA per cell (down to 100uA [2]). This has made the spin-transfer torque writing type memory [3] a viable and serious candidate for low power non-volatile RAM, or universal memory. We demonstrate the circuit and array technologies for a 1.8-V 2-Mb SPRAM (SPin-transfer torque RAM) chip [4].

The feature of spin-transfer torque writing is the direction of current itself through a memory cell determining writing information to the cell, and cell writing current and writing time are comparatively symmetrical between "1" and "0". Thus, the write driver needs to have symmetrical bi-directional current flow capabilities, *i.e.* current source and current sink. We built up a compact bit-by-bit bi-directional current write circuits to achieve proper spin-transfer torque writing of 100ns. For reading, since the read path of memory cell is the same as the write one, read disturbance is the issue. This read disturbance is occurred when anti-parallelized state (high resistance) is read out by parallelizing current direction, and the parallelized state (low resistance) is read out by anti-parallelizing current. We studied the relation between read disturbances and read current direction at high resistance and low resistance states of TMR device. As a result, we developed a parallelizing-direction current reading with 0.7-V bit-line voltage to immune read disturbance that leads to 40ns access time.



Density		2 Mb
Process		0.2 um CMOS, 1 Poly, 4 Metal
Memory Cell size		1.6 um x 1.8 um (designed under 0.4um upper metal L/S)
Power Supply		1.8 V
Write	Cell Current	200 uA
	time	100 ns
Read	time	40 ns
Chip Module size		5.32 mm x 2.50 mm

Fig. 1. Chip Photo and Features

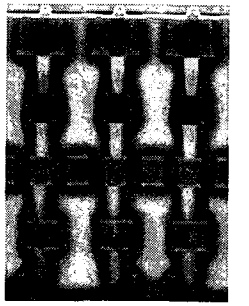


Fig. 2. Cross Section

Chip photograph and its features, using these circuit technologies, are shown in Fig. 1. The chip is fabricated with a 0.2-um logic process and the memory cell is designed using upper metal of 0.4um line and 0.4um space rule (Fig. 2). The MgO thickness is 1.0 nm and the free layer is made of CoFe(1.0nm)/NiFe(2.0nm). No degradations of high and low resistance states are observed after 109 cycles.

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