The Characterization of Poly-Si Thin Film Transistor Crystallized by a New Alignment SLS Process

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Abstract

In this paper, we present work that has been carried out using the SLS process to control grain boundary(GB) location in TFT channel region and it is possible to locate the GB at the same location in the channel region of each TFT. We fabricated TFT by applying a new alignment SLS process and compared the TFT characteristics with a normal SLS method and the grain boundary location controlled SLS method. Also, we have analyzed degradation phenomena under hot carrier stress conditions for n-type LDD MOSFETs.

1. Introduction

Polycrystalline Silicon thin-film transistors(poly-Si TFTs) have been very attractive for the integration of driver circuit into microelectronic applications such as active matrix liquid crystal displays(AMLCDs) and organic light-emitting diodes(OLEDs). In order to improve the TFT device performances, various crystallization schemes have been proposed. Among them, SLS(Sequential Lateral Solidification) technique has attracted a considerable attention due to its excellent throughput and high field-effect mobility.[1, 2, 3, 4, 5]

However, using the SLS technique to manufacture OLED devices, grain boundary(GB) location in channel region of SLS process varies between the TFTs and it results an image quality deterioration of the panel. Therefore grain boundary location control in channel region is an important factor to improve the uniformity and performance of the TFTs, which enhances the image quality of the OLED panel.

In this work, we carried out a grain boundary location controlled SLS method by applying a new key recognition alignment crystallization and it is possible to locate the GB at the same position in the channel region of each TFT.

2. Experimental

Process Ⅰ

Top gate n-channel poly-Si TFTs were fabricated on SiO_2/ SiNx (300 nm/100 nm) which was stacked as a buffer layer on NEG glass substrate. A 50 nm-thick amorphous silicon was deposited on the buffer layer by plasma enhanced chemical vapor deposition (PECVD) as the precursor to laser crystallization. Precursor was dehydrogenated in furnace at 430℃. Then, alignment process keys were formed on an amorphous silicon layer by photo-lithography at each corners of the glass substrate. This was the first photo-lithography layer and following processes were aligned with these keys. After that, SLS crystallization (2-shot process) was carried out.

Process Ⅱ: Key alignment SLS process

In the normal SLS crystallization method, we just perform a basic substrate pre-align on the stage and apply a whole substrate area scan. After we complete all the TFT fabrication processes, each TFT has different GB location in channel region. The number of grain boundaries in the channel also varies from one to two, which can cause non-uniform TFT characteristics and image quality deterioration of the panel. This is because

the tilt between the grain boundary and the following gate line cannot be aligned well when applying the normal SLS crystallization method. Therefore, we carried out a grain boundary location controlled SLS method in this work by applying a new key recognition alignment crystallization which is possible to locate the GB at the same position in the channel region of each TFT.

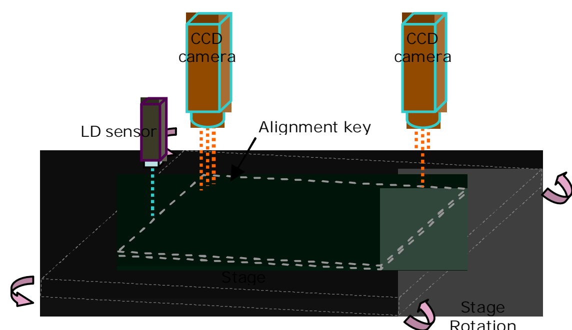


Figure 1. Conceptual image of new key alignment SLS process

Figure 1. shows a concept of a new key alignment SLS process. It was preformed as follows: 1) Glass is loaded onto a substrate stage. 2) Laser diode sensors detect loaded glass edges and calculate the right stage angle. 3) Stage rotates slightly to the calculated angle.(paralleled to substrate scan direction) 4) CCD cameras search alignment process keys on the glass substrate and system calculates the angle and perform a slight rotation to a correct scanning angle. 5) Whole substrate area laser scanning is performed. This new method of key alignment SLS process enables grain boundary to be aligned more finely to following gate lines so it can be advantageous to have more uniform grain boundary location. If we apply an offset value from the start position of line scanning, we can control the exact location of the grain boundary.

Figure 2. shows a top view of SEM image(tilted) of TFT channel region with two grain boundaries located. The change in the GB location can affect TFT performances. Using the grain boundary location controlled SLS method, we have crystallized and fabricated poly-Si TFTs with only one grain boundary located at the same position in channel region at a same gate line.

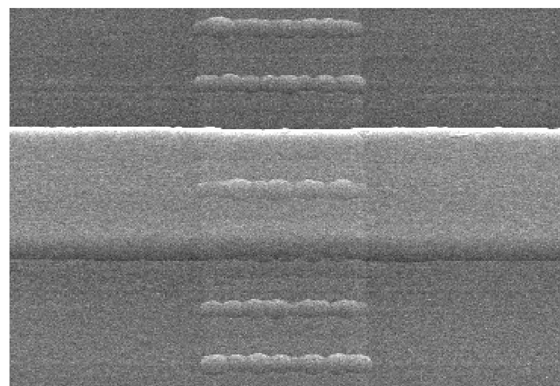
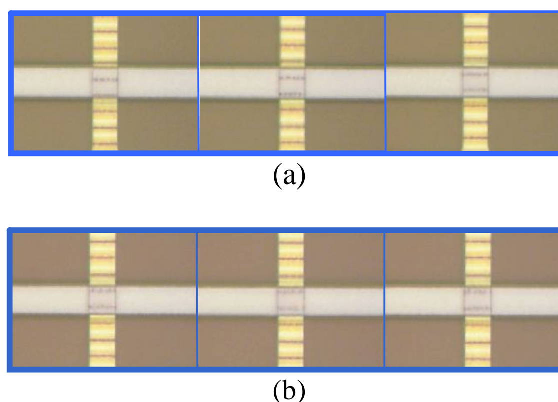


Figure 2. Top view SEM image(tilted) of TFT channel region of one grain boundary located

Figure 3. shows continuous optical images of grain boundary within TFT channel region on the same gate line. As shown in the optical image, there is a change in the grain boundary location within channel region in case of normal SLS crystallization method (a) however, when we apply the grain boundary location controlled SLS method there is no change in grain boundary location within channel region at the same gate lines (b).



(a)

(b)

Figure 3. Optical images of TFT channel (a) when normal SLS crystallization method was applied and (b) when the new alignment SLS crystallization method was applied

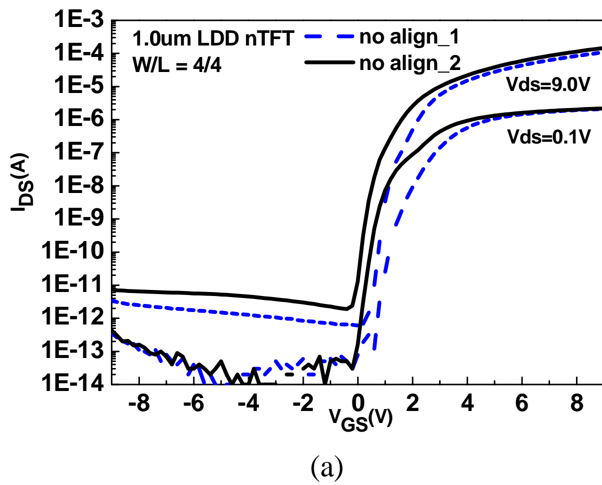
Process Ⅲ

After laser crystallization, active layer was patterned. Gate insulator(SiO_2) of 75nm and gate

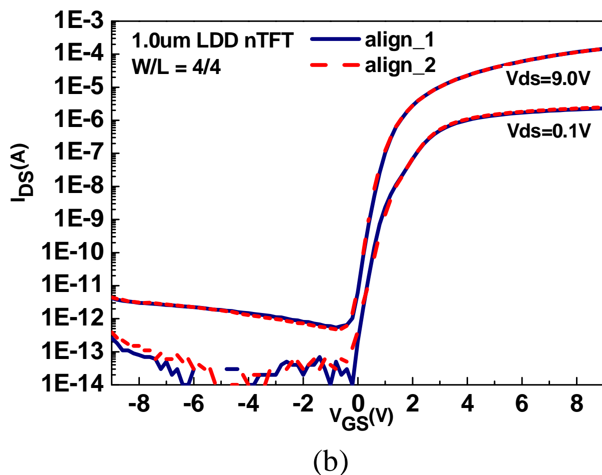
metal(Mo) of 300nm were deposited and patterned. Doping process was carried out in the source and drain region. Source and drain doping concentration was $3x10^{15}cm^{-2}$ for n-type TFT. LDD (Lightly Doped Drain) structure was adopted to reduce the high electric field in the fringe of the drain junction of the poly-Si TFT. Additional nitride(SiNx) layer was deposited for hydrogen passivation. Source and drain metal(Al) of 500nm and ITO were deposited and patterned.

3. Results and Discussion

The transfer characteristics of TFTs were measured at room temperature with V_{ds}=0.1 V and V_{ds}=9.0 V, where the gate voltage(V_g) varied from -9.0 to +9.0 V. We measured TFT characteristics of 1.0 ㎛ LDD (Lightly Doped Drain) n-type TFT(channel width(W)/length(L)= 4 ㎛/4 ㎛)

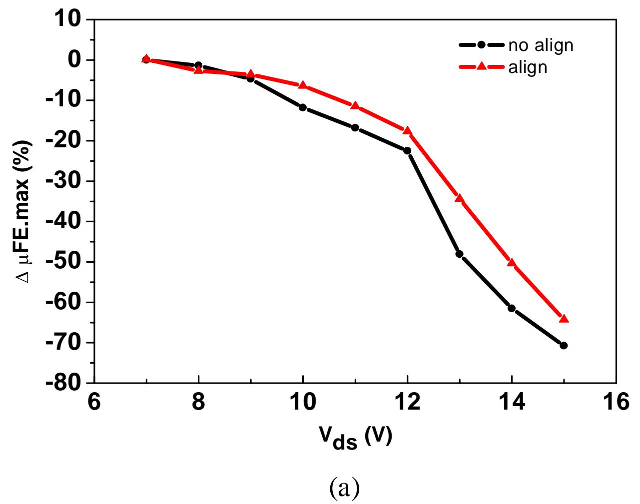


(a)

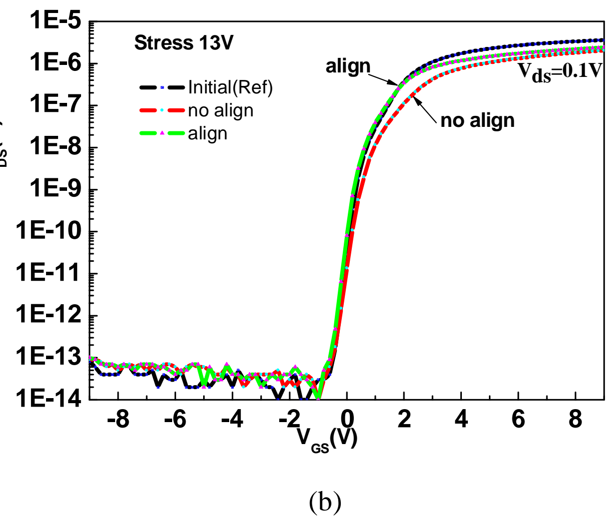


(b)

Figure 4. 1.0 ㎛ LDD (Lightly Doped Drain) n-type TFT device transfer characteristics



(a)



(b)

Figure 5. Comparison of (a)mobility degradation under hot carrier stress and (b)n-type TFT transfer characteristics after stress V_{ds}=13V

Figure 4. shows I_d-V_g transfer characteristics of TFTs crystallized with normal SLS crystallization method. As shown in the transfer curves, when we applied the grain boundary location controlled SLS method, the TFT characteristic showed more uniform performances than with the normal crystallization process. The V_{th} uniformity was improved from 35% to 7%.

In order to examine the alignment crystallization effects on the TFT reliability

characteristics, we measured hot carrier stress(HCS) device performances. Figure 5. shows the comparison of mobility degradation under hot carrier stress as a function of applied V_{ds} with stress duration of 60 sec and n-type TFT transfer characteristics after stress V_{ds}=13V. HCS characteristics of applying the new align method also showed better result than normal crystallization process. As shown in Figure 5 (a), when we applied the grain boundary location controlled SLS method, the Δmobility was decreased about 28% compared with normal process at V_{ds}=13V. In case of applying the grain boundary location controlled SLS method, we found that I_{on} characteristic was higher than the TFT with normal process after hot carrier stress(Figure 5(b)). Therefore, we came to the conclusion that the grain boundary control in the channel region is an important factor to improve the uniformity and reliability of TFT characteristics. As a result, we have accomplished more uniform TFT characteristics than conventional poly TFT by applying the grain boundary location controlled SLS method.

4. Summary

We fabricated a poly-Si TFT using a grain boundary location controlled SLS method by applying a new key recognition alignment crystallization. In this way, it is possible to locate the grain boundary at the same position in the channel region of each TFT. When we applied the grain boundary location controlled SLS method, the TFT characteristic showed more uniform performances than the TFT with normal SLS crystallization process. The Vth uniformity was improved from 35% to 7% and also Δmobility characteristic was decreased about 28% at V_{ds}=13V condition. In conclusion, we have accomplished more uniform and reliable TFT characteristics than conventional poly TFT by applying the grain boundary location controlled SLS method. Also, it can be said that control of grain boundary location is an important factor for the image quality improvement of the panel.

5. References

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