Inverted OLED Structure for 3.5 inch Full Color AMOLED Display on a-Si TFT Backplane

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Abstract

Top-emission 3.5 inch qVGA IOD (Inverted AMOLED) was fabricated with inverted EL structure driven by a-Si TFT backplane. In order to get stable driving TFT, we used FCP(Field Control Plate) layer which was connected with the source of the driving TFT. And we developed planarization process to planarize the cathode layer which was the bottom layer of inverted OLED. Our unique IOD structure is "a-Si TFT/ Al(Cathode)/ LiF/ LG-201(ETL)/ EML(RGB)/ HTL/ LG-101(HIL & Buffer layer)/ IZO (Anode)". LG-201(ETL) layer was studied for more efficient electron injection from cathode to EML, and LG-101(HIL & Buffer layer) covered by IZO anode was also explored for decreasing the EL surface damage.

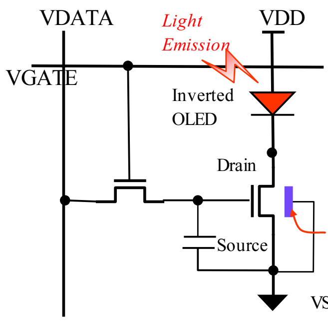
1. Introduction

Active-matrix organic light emitting diode (AMOLED) displays have attracted much attention due to its superior characteristics in flat panel displays such as excellent image quality, fast response time and wide viewing angle. Hydrogenated amorphous silicon (a-Si:H) has also been studied for driving elements of AMOLED displays which employ at least two transistors in a pixel, one is switching transistor and the other is driving transistor. The switching transistor (TFT) is generally operated in the linear region, on the other hand the driving transistor is operated in the saturation region. The driving transistor is required to have large width to length (W/L) and high mobility to supply sufficient current to OLED. But, the a-Si:H transistor with large width to length ratio normally has the poor saturation characteristics.

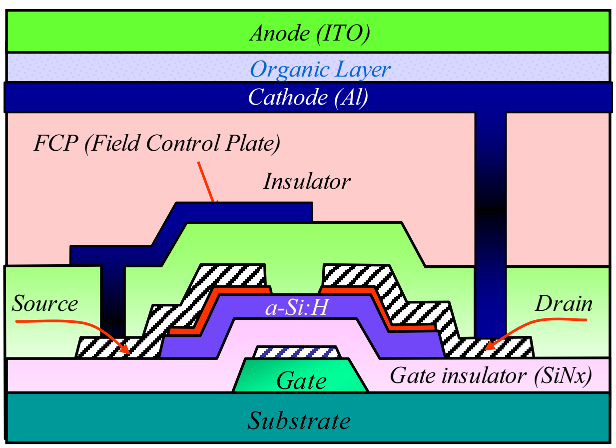
In this paper, we proposed the complemented FCP structure with good saturation characteristics and developed 3.5" full color AMOLED panel with inverted OLED structure.

2. Complemented FCP TFT structure

Figure 1 shows the complemented FCP structure. The a-Si:H TFT with the structure of back channel etched type is used for the switching and the driving transistor. The field control plate is connected with the source of the driving transistor and covers the channel region of the driving transistor. And the cathode electrode of OLED is connected with the drain of the driving transistor, which is the electrode of the inverted OLED structure and covers entire region of the driving TFT. The FCP plate and the cathode electrode play complementary role of control the depletion length and the gradient of carrier concentration of the driving TFT which is controlled by gate to source and drain to source electrodes.



(a) One PXL schematic

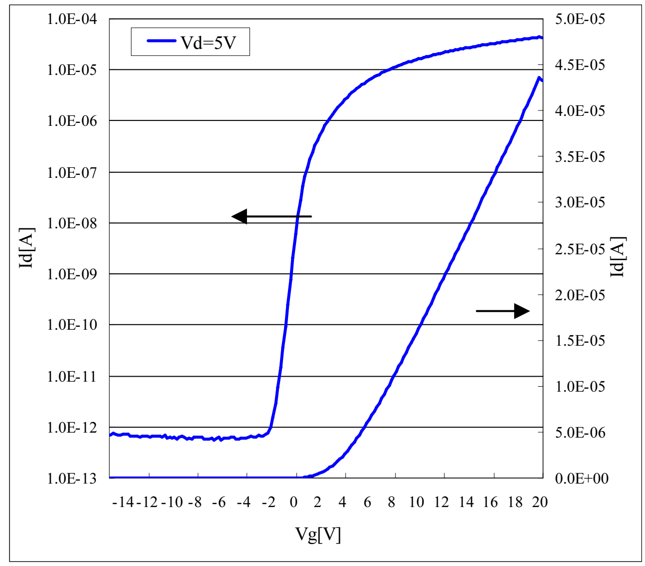


(b) Cross sectional view

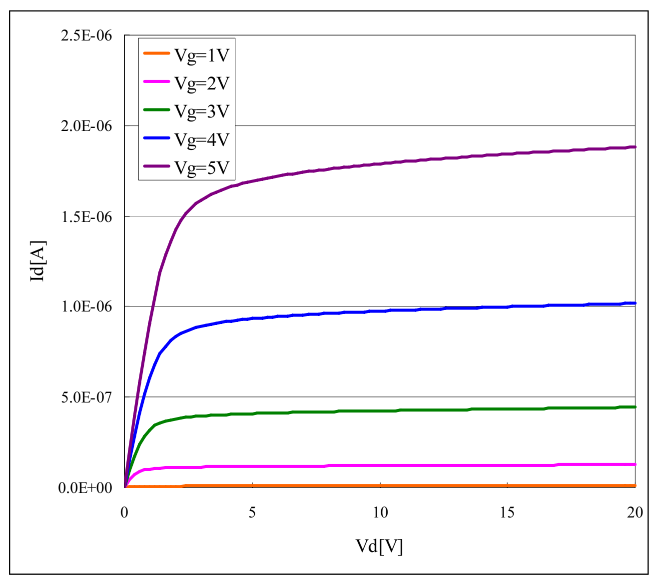
Fig. 1. The complemented FCP TFT structure

The current of transistor is determined by the control of the schottky barrier of the source and the depletion region of the drain. The control of the schottky barrier affects the carrier concentration of the channel and the control of depletion region affects the impedance of the transistor [1]. The FCP connected with source and the cathode connected with drain not only cause the negative shift of the flat band voltage of the semiconductor and the insulator as shown in Fig. 2. (a)., but also makes the change of the distribution of the potential in the semiconductor more wide into high impedance of the channel in the transistor.

Fig. 2 (b) shows the output characteristics of the complemented FCP TFT. The width to length of the driving TFT is 340um/5um. The FCP covers the 3.5um of 5um channel length. In spite of large W/L, the output curve shows the good saturation characteristics and fast increase of the current in the low Vds region by the control of the FCP and the cathode. We can get the stability of the driving TFT with complemented FCP structure.



(a) Vg-Id characteristics



(b) Vd-Id characteristics

Fig. 2. Electrical properties of IOD TFT

3. TFT planarization

We deposited planarization layer on TFT to planarize cathode metal layer which was bottom layer of inverted OLED. The thickness of planarization layer is 1.2 ~ 1.8 μm. The plasma treatment on planarization layer or interposition of buffer layer between the planarization layer and cathode layer improved the adhesion between the planarization layer and cathode metal layer. Fig. 3. cross sectional view of planarization layer.

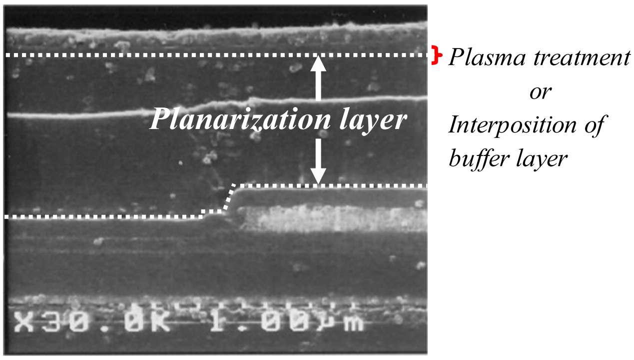


Fig. 3. SEM image of planarization layer.

4. Inverted OLED Cell Performance

Fig. 4. shows the inverted OLED cell structure. The inverted OLED structure had two main issues. One was the damage of EL layer during anode deposition by using DC sputter [2][3], and the other was the low efficiency of electron injection caused by oxidation of cathode [4]. In order to get high performance inverted OLED, we had to solve these two problems.

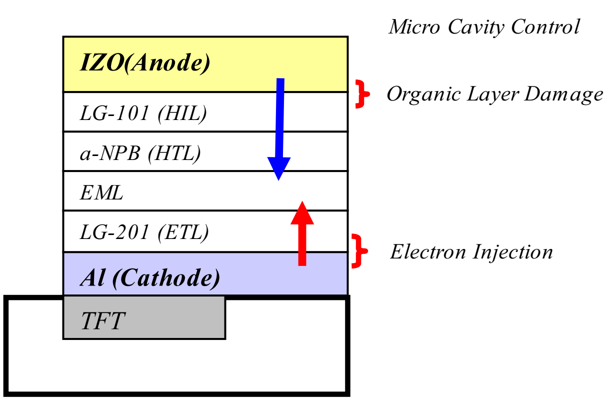


Fig. 4. Inverted OLED cell structure

In order to reduce the damage of EL layer during anode deposition by DC sputterring, we used LG-101 as HIL and IZO as anode electrode. LG-101 has high degree of crystallization and its efficiency of hole injection is high. So LG-101 was used as protection layer between HTL and anode electrode. IZO was also deposited in room temperature for the reduction of the damage of EL layer.

And LG-201, which had good electron injection characteristics was used as ETL to increase the efficiency of electron injection from cathode to EML. We used fluorescence material as blue and green EML, and phosphorescence material as red EML. Generally, hole blocking layer is used in phosphorescence EML structure to prevent the diffusion of triplet exciton from EML to ETL. But we could have high efficiency of electron injection without the hole blocking layer. Table 1. and Fig. 5. show inverted OLED cell performance.

Table 1. R,G,B OLED Cell performance

	@10mA/cm2		Color Coordinate	
	Voltage	Cd/A	(x)	(y)
Blue	4.4	5.6	0.13	0.12
Green	3.6	40.1	0.25	0.7
Red	4	20.9	0.64	0.35
Color Gamut			85%	

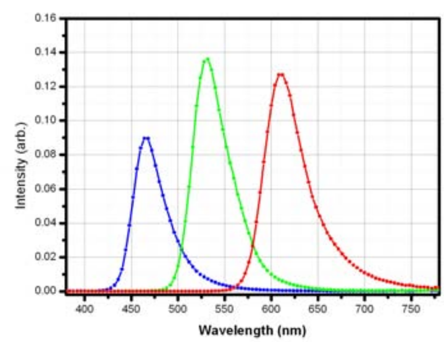


Fig. 5. Emission spectrum of inverted OLED Cell

5. 3.5Inch IOD Panel Performance

We have developed the full color 3.5 inch IOD panel successfully. Table 2. shows the 3.5 inch IOD panel specification and performance. Fig. 6 shows 3.5 inch IOD panel display.

Table 2. 3.5Inch IOD panel specification and performance

Item	Specification
Diagonal Size	3.5"
Emission Type	Top Emission
Resolution	240(H) × RGB × 320(V) Dots
Active Area	53.28(H) × 71.04(V) mm
Dot Pitch	74㎛ × 222㎛ (114ppi)
Number of Colors	R/G/B 256 Gray Level (8 bit)

Item	Performance
White luminance	500 cd/㎡
Vdd	6.2V
Idd	110mA
Power Consumption (30% On)	205mW

Fig. 6. 3.5Inch IOD panel display

6. Summary

We have developed 3.5 inch IOD panel with a-Si TFT backplane widely used in LCD industry. We could get the stability of the driving TFT with complemented FCP structure. To deposit inverted EL on TFT directly, we developed TFT planarization process. We used ETL(LGC-201) to improve electron injection and also HIL(LGC-101) to prevent the damage of the IZO sputtering process. By using a-Si TFT backplane and inverted EL structure, we developed high performance top emission OLED panel. And this OLED structure can be applied to large size AMOLED display.

7. References

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