Development of flexible 3.5" QCIF (176 X144 pixels) OTFT driven OLED : Integration technologies compatible with normal semiconductor processes

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Abstract

Conventional semiconductor processes have been utilized to fabricate 3.5-inch OTFT-driven OLEDs with a resolution of 176 × 144 pixels on plastic substrates. By using a PC-OVD method to deposit a pentacene layer and optimizing patterning and the following processes, we could complete a uniform and reliable integration procedure for an active matrix organic light emitting devices on a plastic substrate. The technical importance of ours is the applicability of conventional semiconductor process to organic materials on plastic substrates. Although there are many hurdles to overcome, our approach and technical improvements are proved to be applicable to plastic electronics.

1. Introduction

Because of its characteristics such as light weight, ruggedness, low-cost and especially a roll-up appearance, flexible display emerges as an ultimate goal for 2-dimensional imaging displays. To bring such a display to reality, three features must be combined and optimized, namely the front planes (LCD, OLED, electronic paper, etc.), back planes (amorphous silicon TFTs, poly-Si TFTs, organic TFTs, etc), and substrates (plastics, metal foils, paper, etc.).

The Organic Thin-Film Transistors (OTFTs) offer many advantages such as mechanical flexibility and light weight compared to traditional field-effect transistors. [1] Amongst many existing switching devices for organic light emitting device (OLED), the OTFT is promising for its compatibility with low temperature processes on plastic substrates.

We hold an opinion that the combination of organic light emitting device (OLED) and organic thin film transistors (OTFTs) as switching devices on a plastic substrate would be the most suitable choice for flexible displays with low cost and high performance. Ideally, printing methods for device fabrication seems appropriate. However, printing method is still in immature state and requires an installation of completely new processing facilities. For the time being, we have approached to use the existing semiconductor facilities and processes for a quick launching of the flexible display.

While plastic substrates are flexible, thin, light weight, tough, and so on, their lower degree of dimensional and thermal stabilities have hindered the integrating processes for electrical devices. Moreover, although flexible OTFT-OLED has advantage of low temperature process, it needs many new materials and processes to realize a truly low temperature process. [2-4]

In this article, we present OTFT-driven OLEDs on plastic substrates, which has a dimension of 3.5 inch in diagonal and a resolution of 176 × 144 pixels. We have used conventional semiconductor processes such as a sputtering deposition of metals, photolithography, wet cleaning and etching, and plasma etching for the fabrication of OTFT backplanes. Especially, we have utilized conventional photolithographic and plasma etching methods to pattern the organic semiconductor layers, which is pentacene. The pentacene islands were hardly damaged during the coating of photoresist (PR) and patterning of the active layer. Also, it endured the oxygen plasma etching and PR stripping.

After the OTFT fabrication processes, integration of the OLED layer to the OTFT backplane was achieved. Finally, we present the OTFT-driven OLED on plastics substrates. The technical importance lies in the fact

that conventional semiconductor processes are applicable to organic materials supported by plastic substrates. Although there are many hurdles to overcome, our approach and technical improvements are thought to be applicable to the fabrication of various plastic electronics.

2. The Structure of a Pixel – Its Circuit and Processing Scheme -

Our OTFT backplane has a dimension of 3.5 inch diagonal with 176 × 144 pixels (i.e., the pixel dimension of 390 ㎛× 390 ㎛.). The OLED front panel was specifically designed for a top-emission, monocolor (green) type display. A conventional 2T-1C pMOS circuitry was employed. The specification of each component was designed by the scheme of ref. 5. The AMOLED was designed to match OTFT performances of mobility ~ 0.05 V. cm^2/sec, on/off ratio ~ 10^6 and of OLED with the efficiency of ~14 cd/A. For the luminescence of 100 cd/m^2 at V_{dd} =15 V, the width/length ratios of the driving and switching transistors were designed by 340/10 (㎛) and 90/10 ㎛), respectively, and the storage capacitance 2.56 pF. Figure 1 shows the schematic diagram of the pixel.

We employed a coplanar bottom-gate structure for the organic thin film transistors. Figure 2 (a) shows the schematic cross-sectional view of the pixel. Except for electrodes and an etch buffer layer, organic materials were used for all layers. To prevent mechanical failures such as a crack and bending, gate dieletrics and passivation layer which cover the whole area of the device region must be organics.

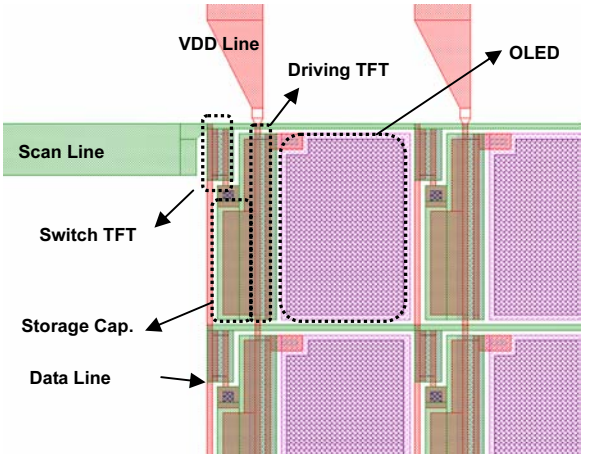
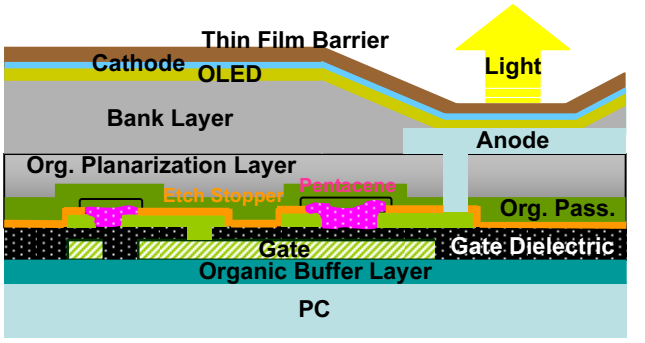
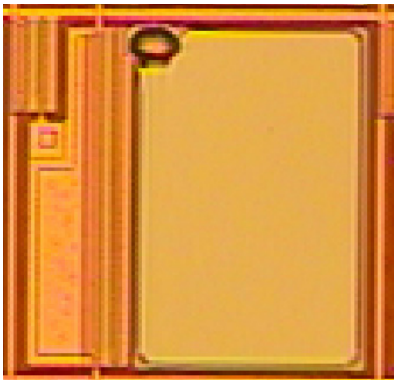


Fig. 1. Schematic Diagram of the pixel structure.



(a)



(b)

Fig. 2. (a) Schematic cross sectional view of the integrated pixel, and (b) Top view of the fabricated pixel.

Figure 2(b) shows the top view of the fabricated pixel followed by the above cross sectional schemes. The aperture ratio was close to 48 %.

3. OTFT-OLED Integration

To maintain a stable, reproducible and semi-automatic processing, we have attached the plastic substrate to a rigid carrier such as a silicon wafer or a glass plate. Both-side adhesive is used for the adhesion of a plastic sheet and a carrier. The peel strength of the adhesive was adjusted to retain adhesion to an extent of which all the processes can be carried out. To facilitate the detachment of the plastic substrate in the final stage, a butyl rubber film was inserted between the adhesive/carrier and the plastic substrate. The butyl rubber is resistant to all solvents which being used in the integration processes, and also does not lose or deteriorate the adhesive strength.

One of the main concerns in handling plastic sheets

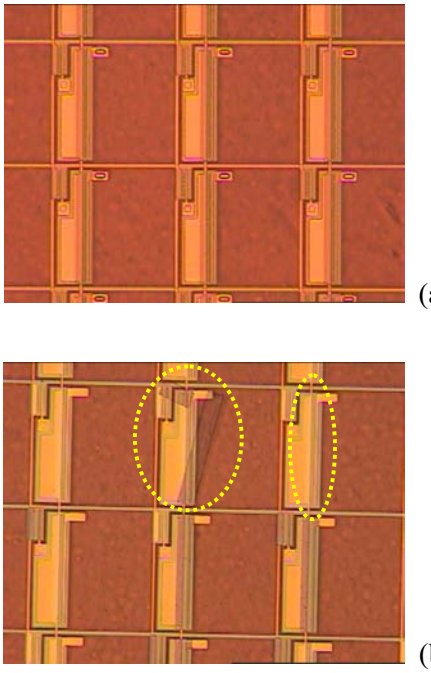
for electronic devices is the particles, which were observed to originating from either the plastic itself or the surrounding. Particles are drawn by static electricity to be placed on the surface of the substrate. Particles attached to the plastic surface are stubborn against being taken away, and causes the problems such as electrical shortage, line failure, and so on. Thus, after achieving a reasonable surface cleanness, we have coated the plastic substrate with a rather thick organic film to bury all residual particles and to planarize the surface.

We used polycarbonate sheets (PC) supplied by Teijin Co. as flexible substrates. All integration processes were kept below 120 ℃. After forming the organic buffer layer, gate electrode (Cr/Al/Cr) was formed. On the electrode, an organic material named SS6908 (JSR) was deposited as an organic gate dielectric by spin coating. The liquid SS6908 was thermally cured to form a stable polymer film, which was subsequently photo-lithographed and O_2 plasma etched to establish contact holes.

After the forming of the source/ drain Au electrodes by a lift-off process, pentacene layer was deposited by a pressure controlled organic vapor deposition (PC-OVD) method, which has been developed independently in laboratory. Figure 3 compares the microscope images of the pentacene islands formed by our equipment and a normal evaporator after the active layer patterning. While pentacene films formed by our PC-OVD method endured the whole pattern process, pentacene films formed by evaporation methods turned out to be vulnerable to PR strip and water cleaning process after normal photolithographic and etching processes. In particular, film peeling occurred with a significant frequency. Based on this observation, we concluded that pentacene thin film deposited by the PC-OVD method is compatible with conventional semiconductor patterning process, which might be attributed to the enhanced in-layer binding of pentacene films.

Double layered parylene were used; one as a buffer layer for the active patterning and another as a passivation layer for the following processes. The parylene layers were deposited by a chemical vapor deposition (CVD) method. No serious damage on the underlying pentacene film was observed, indicating material similarity between two facing surfaces.

As oxygen-plasma was used in our etching process, the selectivity emerges as an important issue to be resolved. In dry etching processes, the film which is subject to patterning is over-etched slightly



(a)

(b)

Fig. 3. Microscope images of the pentacene islands formed by (a) PC-OVD and (b) a conventional thermal evaporator.

to define the pattern accurately. Once the layer beneath is inert to the etching environment over-etching bear no problem. However, as organics are used in nearly all layers, over-etchings with oxygen are very likely to damage the layer which lies beneath. Layers which are damged by over-etching are observed to bring about problems such as gate leakage and/or shortage. In order to protect the lower layer from over-etching, we have formed a shield layer by either depositing an aluminum oxide(AlOx) layer of 30 nm thickness by an atomic layer deposition (ALD) method or spin-coated an SOG layer. The ALD-AlOx layer was grown at the temperature of 100 ℃ and the SOG was cured at 120 ℃ after spin-coating. Our choice of ALD as a method for oxide deposition lies in the fact that, unlike other oxide deposition processes such as sputtering or CVD, by using ALD one can not only form an oxide layer at low temperature but also minimized the occurrence of surface damage of the organic dielectrics. Because SOG was cured at a relatively low temperature, full conversion into silicon oxide was not achieved. However, we find this method as an useful

method to form a shield layer at low temperature. After the formation of shield layer, we have performed wet etching to form the TFT channel. This process deteriorates the characteristics of the OTFT slightly. However, from the processing stability viewpoint, the ALD-AlOx and SOG layers rarely degrade the surface morphology of the gate dielectrics.

We utilized a photocurable polyacrylate polymer as a planarization layer and a bank of an anode for OLED.

Top emission OLED has been fabricated on Cr/Al/Cr anode. To remove any contaminants on TFT array and modify the surface properties of anode, O_2 plasma treatment was performed. The organic layers of NPB (600Å) and Alq3 (600Å) were deposited by thermal evaporation with a shadow mask. The semi-transparent cathode of LiF(10Å)/Al((20Å)/Ag (200Å) was then formed and NPB layer as a buffer layer and IZO layer as a passivation layer were sequentially deposited by evaporation without breaking the vacuum in the same vacuum chamber.

Encapsulation of OTFT-OLED panel was performed with parylene and AlO_x layers fabricated by CVD and ALD) methods, respectively. OTFT-OLED panel was detached from Si substrate and measured the electrical and optical properties.

Figure 4 captures an operating image of a 3.5-inch QCIF OTFT-OLED panel which was fabricated by conventional semiconductor processes at a temperature below 120 ℃.

Fig. 4. An Image of the 3.5 inch OTFT-driven OLED with green emission.

4. Summary

We have developed 3.5 inch AMOLED displays on plastic substrates. The display has a structure of a top emission OLED driven and switched by an OTFT backplane, which has a pentacene active layer. Concerning the integration process of the OTFT and the OLED, various technical improvements have been high-lighted and discussed. Our approach has an advantage of utilizing the conventional semiconductor processing facilities at a temperature lower than 120°C. Although the many technical features are still in progress, our demonstration suggests the feasibility and applicability of our approach to realize flexible AMOLEDs.

5. Acknowledgements

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6. References

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