4.1" Transparent QCIF AMOLED Display Driven by High Mobility Bottom Gate a-IGZO Thin-film Transistors

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Abstract

The authors report on the fabrication of thin film transistors (TFTs) that use amorphous indium-gallium-zinc oxide (a-IGZO) channel and have the channel length (L) and width (W) patterned by dry etching. To prevent the plasma damage of active channel, a 100-nm-thckness SiO_x by PECVD was adopted as an etch-stopper structure. IGZO TFT (W/L=10/50μm) fabricated on glass exhibited the high performance mobility of 35.8 cm^2/Vs, a subthreshold gate voltage swing of 0.59 V/dec, and $I_{on/off}$ of 4.9×10^6. In addition, 4.1" transparent QCIF active-matrix organic light-emitting diode display were successfully fabricated, which was driven by a-IGZO TFTs.

1. Introduction

Recently, transparent ZnO-based TFTs have attracted much attention for flexible displays because they can be fabricated on plastic substrates at low temperature and have the ability to be used to produce highly uniform and large area displays with a low production cost [1]. The Hosono group reported the fabrication of high performance TFTs with amorphous In-Ga-Zn oxide (a-IGZO) channel layers deposited by PVD [1-2]. These TFTs showed a high mobility of >10cm^2/Vs and an excellent subthreshold gate swing (***S***) of 0.20V/dec for a-IGZO TFTs, as compared with those with a polycrystalline ZnO channel, even in the amorphous phase.

Because ZnO-based materials are soluble in wet processes using acid and also vulnerable to plasma damage during dry etching [3], their patterning for process integration is a critical step in the fabrication of TFT arrays. Thus, it is believed that patterning by etching adversely affects the transistor characteristics. Nevertheless, most previous works have focused solely on the improvement of the oxide transistor characteristics: The device performances reported in the literature include field-effect motilities of between 1 and 53 cm^2/Vs and $I_{ON/OFF}$ ratios ranging from 10^4 to 10^8 [1,2,4-11]. Most of the previously reported TFTs have rather large channel lengths and widths (>50μm) because the shadow mask or lift-off techniques were mainly used to pattern the gate electrode, channel, and source/drain electrodes.[1,2,4-11] For real device applications such as high-resolution AM OLED displays (>200ppi), such big TFTs cannot meet the stringent design rule for active matrix displays. Therefore, it is urgent to investigate how patterning by conventional photolithography and dry etching adversely affects the overall device characteristics of a-IGZO TFTs, in order to fabricate TFT arrays with a short channel device (<10 μm) for high resolution AM OLED displays.

In this letter, photolithography and the dry etching process were applied to the formation of an etch-stopper and source/drain electrode. It was found that the adoption of the etch stopper is necessary to prevent plasma-induced damage and to achieve a-IGZO TFTs with high mobility. Moreover, we demonstrate the prototype of 4.1" AMOLED, which is driven by bottom gate a-IGZO TFTs.

2. Experimental

Lithographically patterned MoW (200nm) on a SiO_2/glass substrate with a surface area of 185× 200mm^2 was used as the gate electrode. SiN_x (200nm) film as a gate dielectric layer was deposited by PECVD at a substrate temperature of 330°C. The a-

IGZO film with a thickness of 50nm was grown by rf sputtering on the SiO_2/glass substrate with a surface area of 185×200mm^2, using a polycrystalline $In_2Ga_2ZnO_7$ target at room temperature. The sputtering was carried out at a gas mixing ratio of Ar/O_2 = 65/35 and an input rf power of 450W. The atomic ratio of the IGZO film analyzed by inductively coupled plasma mass spectroscopy was In:Ga:Zn =2.2:2.2:1.0. After defining the a-IGZO channel using photolithography and wet etching, a SiO_x etch stopper was deposited by PECVD and, then, patterned by dry etching using Ar/CHF_3 chemistry. MoW source and drain electrodes (200nm) were formed by sputtering and defined by photolithography, and then patterned by dry etching using SF_6/O_2 chemistry. Finally, the sample was subjected to thermal annealing at 350°C for 1hr. The transfer characteristics of the a-IGZO TFTs were measured at room temperature with an Agilent 4156C precision semiconductor parameter analyzer.

3. Results and discussion

Figures 1(a) and (b) show the schematic cross-section of the IGZO TFTs, which have an inverted staggered bottom gate structure without and with an etch stopper layer (ESL), respectively.

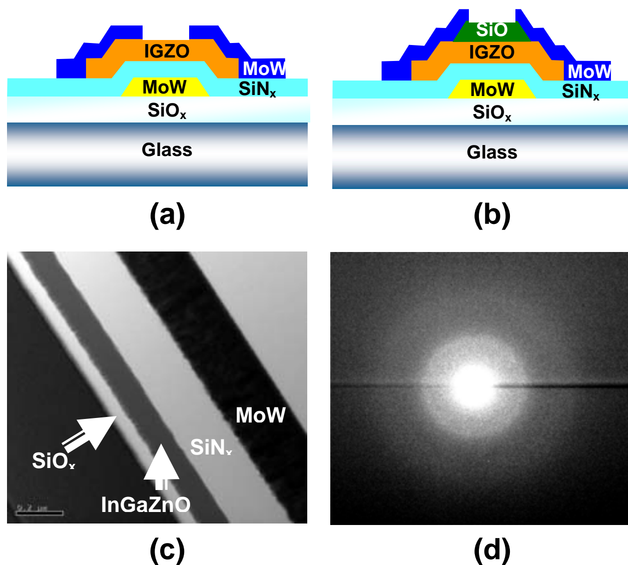

Fig. 1. Schematic cross section of the IGZO TFTs, which have an inverted staggered bottom gate structure, (a) without and (b) with an etch stopper layer, respectively. (c) TEM bright-field image of the stack of SiO_x/IGZO/SiN_x/MoW and (d) the selected area diffraction pattern of the IGZO channel

Figure 1(c) shows the TEM bright-field image of the stack of SiO_x/IGZO/SiN_x/MoW, indicating that the IGZO film is uniform and dense. Figure 1(d) shows the selected area diffraction pattern (SADP) of the IGZO channel layer. The crystalline phase was in the amorphous state and there was no observable microstructure such as a grain boundary.

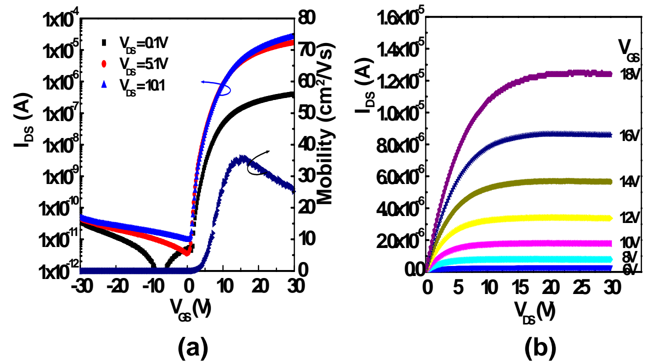

Fig. 2. (a) Representative transfer characteristics of an a-IGZO TFT with W/L=10/50 μm and an ESL. (b) The output characteristics of the a-IGZO TFT with the ESL.

Figure 2(a) shows the representative transfer characteristics of an a-IGZO TFT with W/L=10/50μm and an ESL. The threshold voltage was defined by the gate voltage, which induces a drain current of L/W × 10 nA at a V_{DS} of 5.1 V. The apparent field-effect mobility (μ_{FE}) induced by the transconductance at a low drain voltage ($V_{DS} \leq 1$V) is determined by

$$\mu_{FE} = \frac{Lg_m}{WC_iV_{DS}} \qquad (1)$$

where C_i and g_m are the gate capacitance per unit area and the transconductance, respectively.

For an a-IGZO TFT without an ESL, severe degradations of the field-effect mobility and ***S*** value were observed: the μ_{FE} and ***S*** value were 5.0 cm^2/Vs and 3.5V/dec, respectively. This result can be attributed to the creation of traps due to the plasma damage to the back channel of the IGZO layer during the pattering of the source/drain electrodes. In contrast, the a-IGZO TFT with an ESL exhibited a high μ_{FE} of 35.8 cm^2/Vs, an ***S*** value of 0.59 V/dec, a threshold voltage of 5.9V and an $I_{ON/OFF}$ of 4.9×10^6, as shown in Fig. 2(a). These improvements in the field-effect mobility, ***S*** value, and $I_{ON/OFF}$ ratio of the TFTs with the ESL were reflected in the excellent output

characteristics of the device, which exhibited a clear pinch-off and drain current saturation, as shown in Fig. 2(b).

Figure 3(a) shows the dependence of the channel length on the apparent field-effect mobility of the a-IGZO TFTs. The apparent maximum field-effect mobility of the a-IGZO TFTs decreased from 35.8 to 14.8 cm^2/Vs as the channel length decreased from 50 to 10 μm. In the literature, it was reported that the fringing electric field effects that lead to additional current flow beyond the device edges is responsible for the W/L dependence [12]. However, the fringing electric field cannot be the reason for this because, in our devices, the transistor widths were defined by the active layer width itself. We believe that the a-IGZO transistors are contact limited at short channel lengths. The diminution of the apparent field-effect mobility for short channel devices is due to the existence of parasitic source/drain resistance ($\boldsymbol{R_{SD}}$) on the potential distribution across the channel layer. That is, the externally applied voltages are divided in the channel and source/drain contact regions, due to the non-ideal ohmic contact. Therefore, the magnitude of the actual drain current decreases. As a result, the apparent $\boldsymbol{\mu_{FE}}$ extracted without considering the effect of $\boldsymbol{R_{SD}}$, underestimates the true field-effect mobility. This effect is more serious for short channel devices, because their smaller channel resistance makes the effect of the voltage drop on the contact resistance larger.

In order to estimate the true channel mobility, the $\boldsymbol{R_{SD}}$ was extracted by using the following relationship for the mobility:

$$\mu_{FE} \approx \mu_0 \frac{L}{L + \mu_0 W C_i R_{SD} (V_{GS} - V_T)} \qquad (2)$$

where $\boldsymbol{\mu_0}$ is the true mobility of the a-IGZO material and $\boldsymbol{\mu_{FE}}$ is the apparent field-effect mobility [13-14]. The above equation (2) was used to fit the experimental data in Fig. 3(b). The extracted value of $\boldsymbol{R_{SD}}$ for the a-IGZO TFT was 101 kΩ. Because the channel width is 10μm, the width-normalized $\boldsymbol{R_{SD} \cdot W}$ was 101 Ωcm. Therefore, the true channel mobility for a-GIZO transistor was extracted to 37.9 cm^2/Vs.

The $\boldsymbol{R_{SD}}$ of the a-IGZO TFTs was also calculated by determining the device on-resistance ($\boldsymbol{R_{ON}}$) from the linear region of the transfer characteristics and plotting the width-normalized $\boldsymbol{R_{ON} \cdot W}$ as a function of the channel length for different gate voltages [15]. The inset in Fig. 3(b) shows the device $\boldsymbol{R_{ON} \cdot W}$ as a function of $\boldsymbol{L}$ at V_{DS} = 5.1V for the a-GIZO TFTs. The $\boldsymbol{R_{SD} \cdot W}$ for the a-IGZO TFTs, which is extracted at the y-axis intercept of the extrapolated linear fit of $\boldsymbol{R_{ON} \cdot W}$ versus $\boldsymbol{L}$, is approximately 113 **Ωcm** for V_{GS}=25V. It can be shown that $\boldsymbol{R_{SD} \cdot W}$ itself was a function of the gate voltage: the observed behavior wherein the gradual reduction of $\boldsymbol{R_{SD} \cdot W}$ tails off at a higher gate voltage was also reported for organic TFTs having a large contact resistance [15]. As shown in the inset of Fig. 3(b), a similar $\boldsymbol{R_{SD} \cdot W}$ value (113 Ωcm) was obtained using the transmission line method, indicating that the dependence of the channel length on the apparent field-effect mobility originates from the $\boldsymbol{R_{SD}}$.

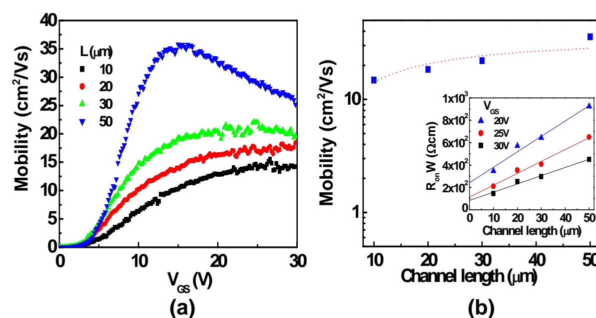

Fig. 3. (a) Dependence of the channel length on the apparent mobility of the a-IGZO TFTs. (b) The extracted field-effect mobility as a function of channel length and the fitting result considering the R_{SD}: the inset shows the device $R_{on}W$ as a function of L at V_{DS} = 5.1V.

Figure 4 shows the display image of 4.1 inch AMOLED display, which was driven by bottom gate a-IGZO TFTs. The developed display has the pixel number of 176 × RGB × 220 at the resolution of 69 ppi. Its sub-pixel pitch is the 123 × 369 μm^2 with the aperture ration of 31% and the pixel element of two transistors and one capacitor. In order to emphasize the transparency of a-IGZO TFTs, the both top and bottom emitting transparent OLED structure was adopted: the semitransparent cathode and transparent anode were used in order to emit the light in the direction of top and bottom. It is noted that the turn-on voltage in top-only emission OLED device is higher than that in bottom-only emission, which is due to the semitransparent electrode. Thus, the transparency of the cathode determines the ratio of the light between top-side and bottom-side. Because the luminescence efficiency of top-side device is less than that of bottom-side approximately by two times, the aperture

ratio of top-emission was designed to 60% to guarantee the same peak luminescence. The transmittance of the AMOLED panel was more than 20%. The higher aperture ratio in the device and higher transmittance in the semitransparent cathode will give the high transparent device. Our demonstration of transparent AMOLED by using a-IGZO TFTs confirmed the applicability of transparent AMOLED in the wide range of new uses, for example, an architectural windows for home entertainment and teleconferencing purposes, auto-motive windshields for navigation and warning systems, and novel helmet-mounted or "heads-up" systems for virtual reality, industrial and medical applications.

Fig. 4. Display image of transparent 4.1inch QCIF AMOLED driven by a-IGZO TFTs.

4. Summary

In summary, the a-IGZO TFT fabricated with an etch stopper exhibited a high field-effect mobility of 35.8 cm^2/Vs, an S value of 0.59 V/dec, and an $I_{on/off}$ ratio of 4.9×10^6. The effect of the channel length on the field-effect mobility was investigated. The apparent maximum μ_{FE} of the a-IGZO TFTs was reduced from 35.8 to 14.8 cm^2/Vs with decreasing channel length. The drop of the apparent field-effect mobility in the short channel device was due to the existence of R_{SD} (~101 kΩ with a channel width of 10 μm). By using bottom gate a-IGZO TFTs as a backplane, we successfully fabricated 4.1” QCIF AMOLED panel, which had the capability of both sides emission and transparency (>20%).

5. References

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