Fabrication of Flexible OTFT Array with Printed Electrodes by using Microcontact and Direct Printing Processes

Jeongdai Jo[1], Taik-Min Lee[1], Dong-Soo Kim[1], Kwang-Young Kim[1], Masayoshi Esashi[2], and Eung-Sug Lee[1]

[1]Intelligent & Precision Machinery Research Division, KIMM, #171, Jang-dong, Yuseong-gu, Daejeon, 305-343, Korea

TEL:82-42-868-7162, e-mail: micro@kimm.re.kr.

[2]Dept. of Nanomechanics, Graduate School of Engineering, Tohoku University, 6-6-01 Aza Aoba, Aramaki Aoba-ku Sendai, 980-8579, Japan

Keywords : microcontact printing, direct printing, organic thin film transistor, printed OTFT, h-PDMS stamp

Abstract

Printed organic thin-film transistor(OTFT) to use as a switching device for an organic light emitting diode(OLED) were fabricated in the microcontact printing and direct printing processes at room temperature. The gate electrodes(5µm, 10µm, and 20µm) of OTFT was fabricated using microcontact printing process, and source/drain electrodes (W/L=500µm/5µm, 500µm/10µm, and 500µm/20µm) was fabricated using direct printing process with hard poly(dimethylsiloxane)(h-PDMS) stamp. Printed OTFT with dielectric layer was formed using special coating system and organic semiconductor layer was ink-jet printing process. Microcontact printing and direct printing processes using h-PDMS stamp made it possible to fabricate printed OTFT with channel lengths down to 5µm, and reduced the process by 20 steps compared with photolithography. As results of measuring the transfer characteristics and output characteristics of OTFT fabricated with the printing process, the field effect characteristic was verified.

1. Introduction

Many of the early demonstrations of conventional inorganic microelectronics made use of a variety of more or less traditional device fabrication techniques for material deposition and patterning, including vapor-phase deposition, photolithography, and wet and dry etching [1, 2]. For other applications, such as those in organic electronics, fiber optics or integrated optical systems that use polymers or sol-gel glasses, these methods have disadvantages: they often require resists, solvents and developers that are incompatible with the materials that must be patterned, they are unable to take advantage of the easy process ability of many organic materials, they cannot be used for single-step patterning of large areas, and they do not work well when applied to rough, uneven or curved substrates. Because of these and other limitations, opportunities may exist for patterning techniques that use contact printing, imprinting, molding, low cost forms of near field photolithography, and for methods based on screen printing, or ink jet printing [1, 3]. More recently, a number of techniques have been introduced to the fabrication of OTFT circuits and displays that aim specifically at reduced processes and fabrication cost [4, 5].

In this paper, we report in more detail related work that OTFT have led to the fabrication of printed electrodes and soluble organic transistors on flexible, transparent plastic substrates. We were design and fabrication the printed OTFT which can be fabricated through a microcontact printing [6, 7] and direct printing processes at room temperature, and will be used as a switching device of a printed electro-mechanical system(PEMS). The gate electrode of OTFT was fabricated using microcontact printing, and source and drain electrodes were fabricated using direct printing process with hard poly (dimethylsiloxane)(h-PDMS) stamp. The OTFT with dielectric layer was formed using special coating system, and organic semiconductor layer was ink-jet printing process.

2. Fabrication of Printed OTFT

Depending on the design of the OTFT and the specific materials and processes used to fabrication it, the cost and performance of the TFT can vary substantially. In order to fabricate a high-resolution and large area printed OTFT on a mask made by hybrid microcontact printing(HμCP) [8] process whose dimensions are 5(L)x5(W)x0.9(H) inches, the pattern area of 30mmx30mm was divided into 4 areas and divided by unit device and 4-pixel and 6-pixel array structure with OTFT with differing pattern shapes, channel lengths and widths. The PDMS stamp used in microcontact printing could be categorized into a soft PDMS(s-PDMS) stamp and a h-PDMS stamp, according to a mold materials, a pattern size, and a fabrication method. The fabrication process of the h-PDMS stamp for the high fidelity pattern form of a nano size is similar to that of the s-PDMS stamp, and it was fabricated by using VDT-731((vinylmethylsiloxane) (dimethylsiloxane) copolymer), SIP 6831.1 (platinum-divinyltetramethyl-disiloxane complex in xylene), a reaction catalyst, Fluka 87927, an adhesion fortifier and HMS-301 ((vinylmethylsiloxane) (dimethylsiloxane) copolymer) as mold materials. The h-PDMS stamp size for OTFT is 125mmx125mmx30mm(±2mm), and the channel length is 5μm, 10μm, and 20μm where the line width and the pattern space are different. And then, we used poly(ethylenenaphthalate)(PEN)(Teijin Dupont Films) which thickness is 200um, and surface roughness is 0.6nm, coefficient of thermal expansion(CTE) is 20ppm/℃ at 200℃, thermal shrinkage is 0.02% (150℃x30min.). The parylene-C was used as organic dielectric layer. The parylene-C of which dielectric strength is 5600(DC volts/mil short time), sheet resistance is 10^{14}(Ω, 23℃, 50%), and dielectric constant is 3.15(60Hz), has the excellent conductive characteristics. Organic semiconductor using pentacene made it OMBD(Organic Molecular Beam Deposition), and poly(3-hexylthiopene-2,5-dily) (P3HT) 0.2w% in chroloforum made it possible to process ink-jet printing. In order to fabricate printed OTFT, we deposited 1000Å of ITO(indium tin oxide) as etching layer using e-beam deposition device on a PEN plastic substrate, and inked hexadecanethiols(HDT) self-assembled monolayer (SAM)(Aldrich) solution up to h-PDMS stamp, transferred into PEN substrates through microcontact printing, and formed single layers, selectively etched ITO using LCE-12K(Cyantek) solution and fabricated gate electrode. On the fabricated gate electrodes, organic dielectric layers of 4300Å, 5000Å, 5600Å, 6500Å, and 7500Å were formed by parylene-C at room temperature using specialized deposition coater, and then carried out lithography process using gate mask and developed. The patterned organic dielectric layer was selectively etched using O_2 plasma for about 10minutes. And on the parylene-C organic dielectric layer, we made 5μm, 10μm, and 20μm of channel lengths(L) and carried out patterning of source and drain electrodes using the h-PDMS stamp, and then it was contacted physically, and an ink injection hole was created in the h-PDMS stamp. The source and drain electrodes were formed by the direct printing process wherein low viscosity as 4cps(at 22℃) and low resistance (0.084Ω/sq/mil(25μm)) conductive Ag ink was injected. And on the contact electrodes, we were deposited organic semiconductor layer using e-beam deposition(HELISYS) whereby the vacuum deposition is carried out 1000Å thickness under the condition of keeping at rate of 0.5Å/sec and 450Å thickness under the condition of keeping at rate of 0.3Å/sec, and ink-jet printing of P3HT by 10times at 100μl using an ink-jet system(UNISYS). Figure 1 show fabrication process of printed OTFT by using microcontact printing and direct printing processes. In the fabrication of OTFT, microcontact printing and direct printing processes have been used to pattern gate electrodes, gate dielectrics, and source and drain contacts with sufficient yield to allow the fabrication of several hundred transistors.

3. Experiment and Results

OTFT is required to reduce the operating voltage less than 5VDC for plastic electronics and flexible display [1]. We have two approach methods such as decrease the channel length and the thickness of gate dielectric. For the fabrication of the printed OTFT on the flexible substrate, the gate electrode of the printed OTFT was fabricated using the microcontact printing process with the h-PDMS stamp onto which SAM used as an etching mask was applied selectively. The source and drain electrodes were fabricated using the direct printing method whereby the h-PDMS stamp is physically contacted on the base layer by injecting low viscosity conductive ink. The organic dielectric layer was coated at room temperature and the organic semiconductor layer was formed by ink-jet printing process. During the OTFT fabricating process, in order to keep the flatness, we used film photoresist (DFR) as adhesion layer and glass substrate as rigid layer adhered to PEN substrate layer. Then put the glass substrate on the hot plate maintained at 60℃, cut the DFR film in proper size, and adhered closely flattening out using roll laminator and then, adhered PEN film to the glass substrate without passivation layer on the hot plate. Figures 2(a) and (b) show the actual h-PDMS Stamp and printed OTFT devices fabrication using microcontact printing and direct printing processes on the 5 inch PEN substrate with channel lengths were 5µm, 10µm, and 20µm, where the line width and the pattern space were different. The h-PDMS stamp with a high resolution corresponds exactly to the mask pattern, and could be replicated a pattern up to the size of 600nm(not shown here). In figure 2(c) shows the optic microscope image of a printed OTFT array with channel length L=20µm and width W=500µm, and pentacene as the semiconductor, 7000Å coated parylene-C as the gate dielectric layer at room temperature, ITO coated PEN film as the gate electrode, and Ag source and drain electrodes, and figure 2(d) shows the device fabricated by P3HT as the semiconductor using ink-jet printing process, 5600Å coated parylene-C as the gate dielectric layer. In the case of printed OTFT as shown in figure 2, it was fabricated without any defect for the pattern sizes of 5µm, 10µm, and 20µm, but it could be ascertained that for the kind of Ag ink and the way of injection, the formation was poor and a number of defects took place so that the pattern was hardly transferred as shown in figure 3. It could be known that a phenomenon that printed OTFT wasn't completely formed took place due to the effect of the contact between the h-PDMS stamp and the PEN substrate. It is required to optimize the surface treatment process, the method of injection process, and the fabrication process including the curing temperature and the curing time in a novel method. And, parylene-C was used as organic dielectric layer, and was formed at 0.1torr and room temperature. The thicker an organic dielectric, the rougher of surface, and a rough channel/dielectric interface had negative effects on performance. We have used a SAM of 1-hexadecanethiol to modify the surface energy of the Ag electrode in an effort to improve the crystal size and ordering of the organic semiconductor over growth. Figures 4 and 5 show the measurement results of the transfer characteristics of the printed OTFT with P3HT. Figure 4 shows a typical plot of drain current I_D versus drain voltage V_D at various gate voltages V_G, which corresponds to a device using pentacene as the semiconductor, 7000Å coated parylene-C as the gate dielectric layer at room temperature, ITO gate, and Ag source and drain electrodes. Figure 5, which corresponds to figure 4, shows such a plot, and channel length was equal to 5µm and width was equal to 500µm. As a result of conducting the OTFT fabricated with soluble P3HT, the performance showed that the on/off current ratio was 1.26×10^3 and that the off current was 1.26×10^{-10}A. Printed OTFT devices were fabricated using an all room temperature process. Additionally, we demonstrated full compatibility with transparent plastic substrates by fabricating devices on PEN substrates, so that it was possible to minimize CTE and to provide better alignment in the patterning process. Besides, since there was no substrate deformation, it was possible to prevent property degradation.

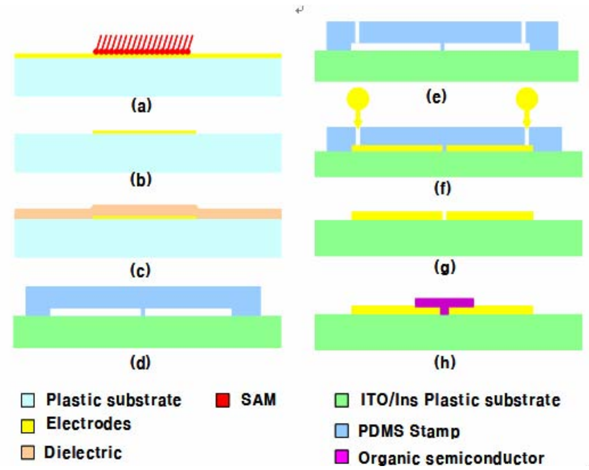
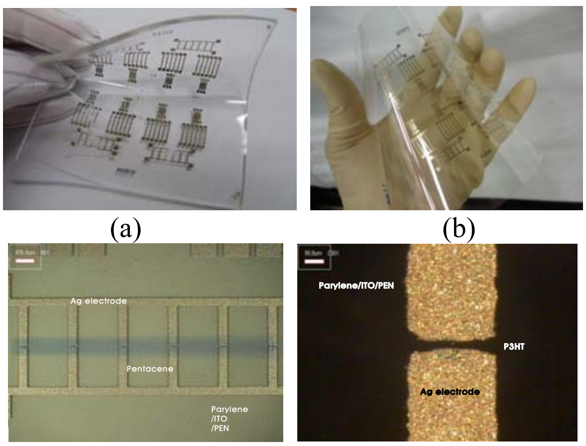


Fig. 1. Fabrication of OTFT using microcontact printing and direct printing processes (a) Inked SAM solution on ITO deposited PEN substrate, (b) fabricated gate electrode, (c) deposited and patterned dielectric layer, (d) physical laminated on ITO and parylene formed PEN substrate, (e) fabricated injection hole, (f) injected conductive ink, (g) fabricated source and drain electrode, and (h) jetting organic semiconductor

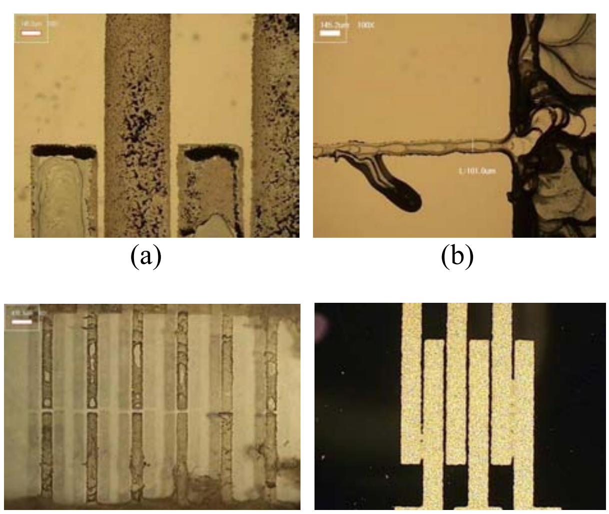
4. Conclusion

Microcontact printing and direct printing processes using SAM, h-PDMS stamp, and low viscosity conductive ink made it possible to enhance the accuracy of classical printing to a precision comparable with photolithography, creating a low-cost, large-area, high-resolution patterning process. Also, printed OTFTs were fabricated using an all room temperature process, there was no appeared such as pattern shrinkage, pattern transformation and bending problem. Also, h-PDMS stamp has a replicated pattern exactly corresponding to the master pattern and has a high accuracy of filling and releasing. As results of measuring the transfer characteristics and output characteristics of the printed OTFT fabricated with the printing processes, the field effect characteristic was verified. Once the surface treatment and process conditions have been improved, this process in place of the conventional photolithography process can make an important use in the drive device of flexible display.



(a) (b) (c) (d)

Fig. 2. Results of OTFT fabrication: (a), (b) 5" size h-PDMS stamp and printed OTFT with channel lengths of 5µm, 10µm, and 20µm(width=500um) on PEN substrate, (c) pentacene printed OTFT with parylene-C dielectric layer, ITO gate, and Ag source and drain electrodes using conductive Ag ink, and (d) P3HT printed OTFT on PEN substrate



(a) (b) (c) (d)

Fig. 3. Results of failures and defects in printed OTFT fabrication: (a) infidelity, (b) leakage ink, (c) pinhole, and (d) short of channel

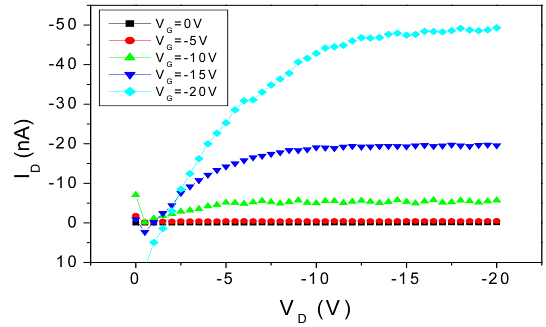


Fig. 4. I_D-V_D output characteristics of printed P3HT OTFT(W/L=500µm/20µm) *(collaboration with J.B. Koo, ETRI)*

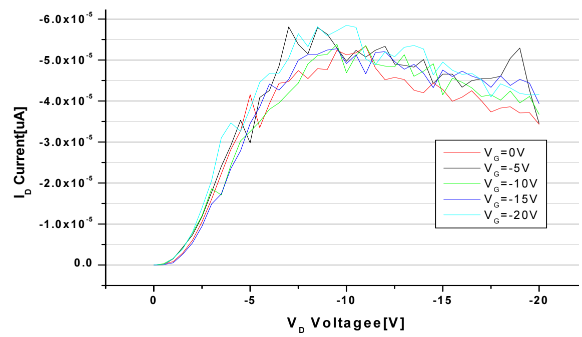


Fig. 5. I_D-V_D output characteristics of printed P3HT OTFT(W/L=500µm/5µm)

5. References

1. J.G. Lee, Y.G. Seol, N.-E. Lee, Thin Solid Films, Vol. 515 No. 2 (2005), p. 805.
2. Fengliang Xue, Zhengchun Liu, Yi Su, Kody Varahramyan, Microelectronic Engineering, Vol. 83 (2006), p.298.
3. C. D. Dimitrakopoulos, D. J. Mascaro, IBM J. Res. & Dev., Vol. 45 No. 1 (2001), p.11.
4. H. Klauk, Thomas N. Jackson: Organic Thin Film Transistors, Molecular Nanoelectronics, edited by Mark A. Reed/Takhee Lee, American Scientific Publishers, California, (2003) p.291.
5. J.A. Rogers, Z. Bao, M. Meier, A. Dodabalapur, O.J.A. Schueller, G.M. Whitesides, Synthetic Metals Vol. 115 (2000), p. 5.
6. H. A. Biebuyck, N. B. Larsen, E. Delamarche, B. Michel, IBM J. Res. & Dev., Vol. 41, No.1-2 (1997), p.159.
7. Younan Xia, J. A. Rogers, K. E. Paul, G. M. Whitesides: New methods for fabrication of nanostructures, Chem. Rev. 99 (1999), pp.1823.
8. Jeongdai Jo, Jun-ho Jeong, Kwang-Young Kim, Eung-Sug Lee, KR. Patent 10-2004-0005548, (2004).