Direct Fabrication of a-Si:H TFT Arrays on Flexible Substrates: *Principal Manufacturing Challenges and Solutions*

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Abstract

Principal challenges to direct fabrication of high performance a-Si:H transistor arrays on flexible substrates include automated handling through bonding-debonding processes, substrate-compatible low temperature fabrication processes, management of dimensional instability of plastic substrates, and planarization and management of CTE mismatch for stainless steel foils. Viable solutions to address these challenges are described.

1. Introduction

The Flexible Display Center (FDC) at Arizona State University is a unique partnership vehicle wherein academia, industry, and government collaborate on rapid technology development, innovation and integration to create a new generation of innovative displays that will be flexible, lightweight, low power, and rugged [1]. These revolutionary displays will usher in a new era of powerful real-time information sharing through ubiquitous application in everything from portable human borne or human worn devices, to displays for vehicles, and for permanent or temporary conferencing and command/control rooms.

The mission of the FDC is to dramatically accelerate the commercialization of advanced high information content flexible display technologies through execution of an aggressive Strategic Plan that simultaneously evolves the technology in the dimensions of degree of flexibility, form factor, resolution, lifetime, and a host of other performance specifications, while developing the manufacturing toolsets and processes to fabricate high quality, high technology readiness level (TRL) integrated technology demonstrators (TDs). The Center is focused on integration of amorphous silicon (a-Si:H) on flexible substrates with reflective and emissive technologies that are intrinsically compatible with the flexible format. In the following sections we review the key issues embedded in the different dimensions of the technology development critical path, including automated flexible substrate handling in a Pilot Line environment, flexible substrate compatible low temperature a-Si:H process development, and direct TFT array fabrication on the flexible substrates.

2. Experimental

Flexible display and associated manufacturing technology development is currently conducted on the Center's 6" wafer-scale Pilot Line. Note that Pilot Line scale-up to GEN II display-scale is underway. The 6" line is operated by a dedicated full-time permanent professional staff, and is linked to a *MassGroup* Manufacturing Execution System (MES) that provides a high level of real time integrated information on Lot status and operational capability, and facilitates yield enhancement and troubleshooting.

Fully automated E-test is provided by an FDC custom hardware integration of Electroglas probers with Keithley electronics. Two probers run continuously (24/7) under FDC-custom LabView control to provide detailed I-V characteristic curves for a representative set of TFTs on each substrate and an additional prober is employed to provide TFT array test for uniformity and yield. Cycle time for TFT array fabrication and E-test is 2-3 weeks, thereby allowing many cycles of process improvement aimed at rapidly providing higher performance TFTs at higher yield.

3. Results and discussion

Flexible Substrates and Handling Protocol

From the candidate flexible substrate technology options, the FDC down-selected heat-stabilized PEN (HS-PEN) from *DuPont Teijin Films* (*DTF*) as the preferred low temperature transparent polymer substrate, and thin stainless steel (SS) as the preferred

high temperature, opaque inorganic platform. The HS-PEN has been extensively characterized and benefits from good thermal dimensional stability, low moisture uptake, moderate CTE, and good surface properties. For polymeric substrates, a crucial issue is dimensional stability, which is critical for high yield layer alignment in transistor builds. A key limitation of the HS-PEN material is its upper temperature limit of ~200 °C., requiring us to limit process steps to a maximum temperature of 180 °C.

Stainless steel (SS) foils are attractive candidates because they are inherently impermeable, thereby requiring no environmental barrier layer, and because they can be processed at relatively high temperatures. However, they require a planarizing and electrical isolation layer, and the material employed (typically a low κ polymer such as polyimide or BCB) may introduce its own constraints of dimensional stability, CTE mismatch, moisture absorption, *etc*. A significant liability for SS in the long run is its intrinsic limited flexibility. However, for applications in which rugged and lightweight are the desired display attributes and a rigid planar or conformal display format is desired or acceptable, this limitation is a non-issue.

HS-PEN substrates were provided by DTF and were used as received. For the stainless steel substrate a planarization / electrical isolation layer was deposited on the foils prior to fabrication. In terms of electrical isolation the layer should provide an active area-to-substrate capacitance of < 2 nF/cm^2 and a leakage current to the substrate of < 6 nA/cm^2 at an electric field of 4 x 10^5 V/cm [2-3]. The planarization should reduce the rms surface roughness to < 10 nm while providing good adhesion and acceptable CTE. Wagner and coworkers [4] have recently presented a comprehensive screening study in which spin-on glass (SOG), spin-on polymers and PECVD layers were evaluated for SS planarization and electrical isolation for a-Si:H TFT array fabrication. They concluded that adequate planarization was obtained only for benzocyclobutene (BCB) and SOG, but that SOG layers required an additional PECVD silicon nitride layer to achieve adequate electrical isolation.

The FDC independently conducted a screening study in which over a dozen candidate planarizing/isolation layers were evaluated. Peak-to-peak and rms surface roughness were determined using a VEECO Dimension 3100 IVa AFM in contact or tapping mode. For each wafer results were averaged for nine different 100 μm *x* 100 μm scan areas. Based on screening outcomes, four final candidate materials including BCB, two polyimides from Brewer Science, and a new undisclosed material from FDC member *Honeywell Electronic Materials* were down-selected. Although the BCB material exhibited the best performance quantitatively for local roughness reduction (consistent with the findings reported in [4]), difficulties associated with poor wetting behavior were encountered, which led to undesirable large-length-scale non-uniformity. Moreover, this issue became more severe for planarization of the pre-coated SS. In contrast the *Honeywell* material performed quite well as a planarizing layer for both uncoated and pre-coated SS, and we therefore employed this new material for planarization prior to TFT array fabrication.

To enable the flexible substrates to be processed in our Pilot Line tools that were built to process rigid substrates, we have adopted a temporary bonding / de-bonding approach. This approach requires simultaneous development of new temporary adhesive materials, new or adapted manufacturing toolsets, and associated processes. Principal challenges are as follows: (i) the temporary adhesive must be "semiconductor grade", *i.e*., it must have a total thickness variation that approaches that of a Si wafer, it must be particle-free, and free of impurities that might contaminate the TFTs, and it must be compatible with the full range of TFT fabrication processes; (ii) the bonding processes must be manufacturable (fully automatic, reproducibly yielding bubble-free high integrity bonded layers); and (iii) the de-bonding processes must also be automatic through some form of "triggered" release that results in a debonded flexible substrates without damaging or degrading the performance of the TFT arrays, and without leaving any adhesive residue on the substrate.

We have worked with our bond / de-bond toolset partner *EVG* and adhesive materials partners and suppliers to develop custom bonding solutions for both HS-PEN on Si and SS on Si. Figure 1 shows pictures of a PEN wafer bonded to Si, the bonded wafer after TFT fabrication of a set of 64x64 reflective and emissive TFT arrays, and the flexible PEN after de-bonding. We continue to work to develop the materials and adapt the toolsets to provide fully automatic, manufacturable fabrication processes.

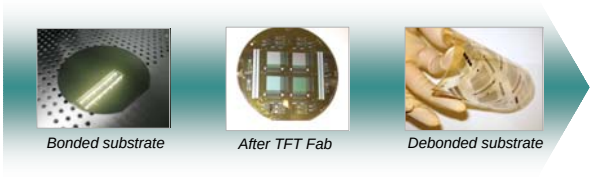

Fig. 1. HS-PEN substrate at different stages of processing: (left) bonded to Si prior to TFT fabrication; (middle) after 64x64 TFT array fabrication; and (right) after debonding

Low Temperature a-Si:H Process

Principal challenges in low temperature a-Si processing are associated with the quality of the materials and interfaces in the active device stack, [5-7] including: (i) higher SiH_2/SiH ratio in a-Si:H, which leads to a higher threshold voltage V_t and a lower saturation mobility μ_{sat}; (ii) greater charge trap density in the a-SiN_x:H gate dielectric, which results in greater electrical stress induces V_t shift (device instability) and hysteresis [7]; and (iii) unactivated dopants and unstable interfaces in n^+ a-Si:H contacts, which gives greater contact resistance and turn-on voltage offset. These challenges are faced in glass-based TFT processes run in the 300 to 350 °C. range, but become more severe the lower the allowed maximum process temperature. Hence completely different process windows from conventional LCD-like TFT manufacturing must be identified to provide near or equivalent transistor performance.

An FDC-proprietary low temperature (180°C) a-Si:H TFT channel-passivated process flow was defined to be intrinsically high yielding and readily scaled to display manufacturing toolsets (*e.g*., GEN II and beyond). Key process development studies encompassed and addressed the issues summarized above, and focused on the a-Si:H channel layer, the silicon nitride gate dielectric layer, and the n^+ a-Si:H contact layer. Each of these processes is run at 180°C; all other processes in the flow are run at lower temperatures. Post-fabrication anneal processes are not employed. As of June 2007, the FDC baseline process produces TFT arrays with statistically averaged μ_{sat} equal to 0.9 cm^2/V-s and ON/OFF ratio greater than 10^9, and with TFT fit yields in the 99-100% range. We continue to work to improve our processes and devices, with a current focus on improvement of interlayer dielectric (ILD) processes.

Direct TFT Array Fabrication on Flexible Substrates

A 3.8" diagonal 320 x 240 QVGA reflective backplane (105 ppi) was designed with design rules for high manufacturing yield on flexible substrates. The transistor design is a bottom-gate inverted staggered trilayer TFT architecture. This mask set was used to fabricate TFT arrays on HS-PEN and SS.

With respect to direct fabrication a-Si:H TFTs on HS-PEN, the principal technical issue to address is that of dimensional stability. In this regard, we have found that dimensional instability due to thermal cycling and material shrinkage (run-in) is not an issue as a consequence of the heat stabilization process. Likewise moisture absorption and swelling of the polymer to cause material expansion (run-out) is also not a serious issue since it can be readily controlled with barrier layers and environmental/process equilibration procedures. Instead the principal issue to be addressed is material run-out due to elastic expansion of the PEN in response to deposition of high stress films. Street and co-workers addressed this problem by developing a low temperature a-Si:H process (150 °C) in which the deposition processes are tuned to produce low stress films [8]. Nathan's group [9] has shown that the crucial silicon nitride gate dielectric layer can be deposited in a process window that produces low stress films, but that this window produces films with a N:Si atomic ratio less than 1.6, and that these films exhibit substantially degraded TFT performance relative to the higher stress nitrogen-rich films with N:Si ratio greater that 1.6 At the FDC we have therefore chosen a path that does not rely on low stress active layer films and the additional constraint on process window that the low stress path introduces. Instead we are focused on modest changes to process to moderately reduce film stress and to balance stresses, while simultaneously working with our substrate partners to modify and improve the substrate material systems to make them less susceptible to run-out. This approach has yielded a 2-3x reduction in PEN run-out for our standard process, with a maximum relative distortion of ~100 ppm. This level is adequate for fabrication of low resolution, small form factor TFT arrays without employing distortion compensation, which must however be employed for high ppi and large form factor arrays.

Figure 2(a) shows a TFT array drive current test map for a QVGA array fabricated on HS-PEN without employing photolithographic distortion compensation. White points on the map indicate shorts; black indicate open pixels. A perfect array would show as an even "deep blue sea" map; the more uniform the shades of blue the more spatially uniform is the TFT performance across the array. Point defectivity is less than 0.2%; the defects are primarily in the form of TFT shorts. The map indicates reasonable uniformity across the array, and optical micrographs visually confirmed good alignment from corner-to-corner. Figure 2(b) is a photograph of the corresponding electrophoretic ink display (EPD) build.

At the GEN II Pilot Line scale we will have the capability to employ active photolithographic distortion compensation to deal with the residual distortion with our Azores 5200gT PanelPrinter™, the world's first installed GEN II photolithography system specifically designed and optimized for manufacturing TFTs on

Fig. 2. (a) Drive current map for TFT array built on HS-PEN; (b) corresponding EPD build.

flexible panels. The tool was developed with partial funding from FDC Principal Member *USDC*, and incorporates *active compensation architecture* (ACA), through which process-induced dimensional distortion is automatically pre-measured and accommodated for during step-and-repeat stitching and layer alignment ("registration") process steps.

Figure 3(a) shows a TFT array drive current test map for a QVGA array fabricated on SS planarized with the *Honeywell* material. Point defectivity for this array is less than 0.5%; the defects are primarily shorts and are likely due to inadequate planarization at asperities in the SS substrates. Balancing the CTE and physical properties of the carrier and temporary adhesive was a key to achieving high quality arrays. Figure 3(b) is a photograph of the corresponding EPD build.

Fig. 3. (a) Drive current map for TFT array built on SS; and (b) corresponding EPD build.

Both the EPD on HS-PEN and the EPD on SS exhibit good performance characteristics, including 4-bit (16 shades) grey-scale; 0.7 s image refresh speed, and good image stability. Work is ongoing to improve yields and display performance.

4. Summary

The FDC has created viable technology solutions for key barriers to manufacturing high information content flexible displays, including:

- Handling protocols for flexible substrate systems based on temporary bonding – debonding
- A low temperature a-Si:H process that produces high performance transistors at good yield
- Processes and protocols for direct fabrication of TFT arrays on flexible substrates

These advances have been demonstrated through fabrication of 3.8" QVGA EPDs on both plastic and metal foil substrates.

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