Design of line memory with low-temperature poly-silicon(LTPS) thin-film transistor (TFT) for system-on-glass (SoG)

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Abstract

A 12k-bit SRAM has been developed for line memory of system-on-glass (SoG) with low-temperature poly-silicon (LTPS) thin film transistor (TFT). For accurate sensing even with the large variation and mismatches in the characteristics of LTPS TFT, mismatch immune sense amplifier is developed. The SRAM shows 30ns read access time with 7V supply voltage while dissipating 4.05mW and 1.75mW for write and read operation, respectively

1. Introduction

With low-temperature poly-silicon (LTPS) thin film transistor (TFT), various kinds of display electronics can be integrated on the same glass substrate as pixel due to its much better performance than amorphous-Si (a-Si) TFT [1]. The ultimate goal of flat panel display with LTPS TFT is system-on-glass (SoG) which has all the display electronics on the glass substrate. However, there are lots of obstacles to be overcome for successful implementation of high-performance and low-cost SoG [2]. One of the most challenging difficulties is the large variation and mismatch in the characteristics of LTPS TFT due to the grain boundaries of poly-Si substrate. These are very critical for analog circuits such as digital-to-analog converter (DAC), source driver, and DC-DC converter [3-7].

Although line memory can be removed by modifying the system interface architecture, line memory built with SRAM is generally required to be integrated on glass substrate as well for SoG [8]. Because the internal signals of SRAM have very small magnitude, the building blocks of SRAM are also very sensitive to the variation and mismatch of LTPS TFT, especially the sense amplifier.

In this paper, a 12k-bit SRAM for line memory of SoG is described which is implemented with a 2μm LTPS TFT technology. Sense amplifier is developed so the mismatch of LTPS TFT is compensated to detect the small voltage difference between the complementary bit lines during the read operation. The next section describes the architecture and circuit design of the SRAM and the simulation results and conclusion follow.

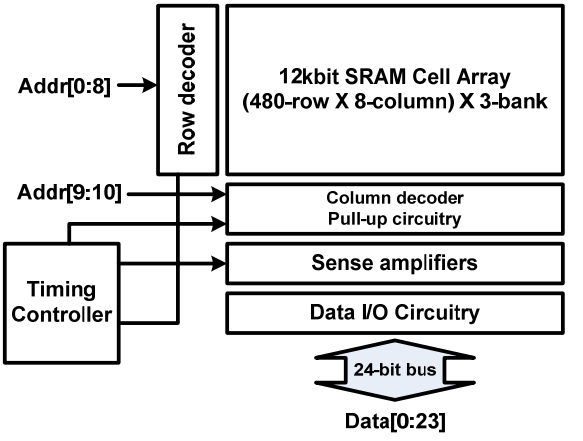


Fig. 1. Architecture of 12k-bit SRAM with LTPS TFT for SoG.

2. Architecture of SRAM

A 12k-bit SRAM is designed for line memory of SoG with VGA format (640 x 480) and 8-bit gray scale. As shown in Figure 1, the cell array comprises 3-banks with 480-rows and 8-columns. Each column has a sense amplifier and data I/O circuitry. The control signals PU_E, READ_E, and WRITE_E are pull-up enable, read enable and write enable signals, respectively.

The detailed cell array configuration of a bank is shown in Figure 2. The conventional 6-transistor SRAM cell is employed. In the LTPS TFT technology used in this work, the driving capability of p-channel TFT is much better than n-channel TFT of same size and therefore the logic threshold voltage of inverter is very high (about 5V with 7V supply if (W/L) of n-

channel TFT is 4 times larger than that of p-channel TFT). Thus, the noise margin for logic HIGH is very small or even negative if n-channel TFT is used for access transistor. Figure 3 shows the transfer characteristic of cross-coupled inverters and the noise margins when access transistors built with n-channel and p-channel TFT. With n-channel TFT, the noise margin for logic HIGH(NMH,N) is negative because of the voltage drop of V_{TN}.

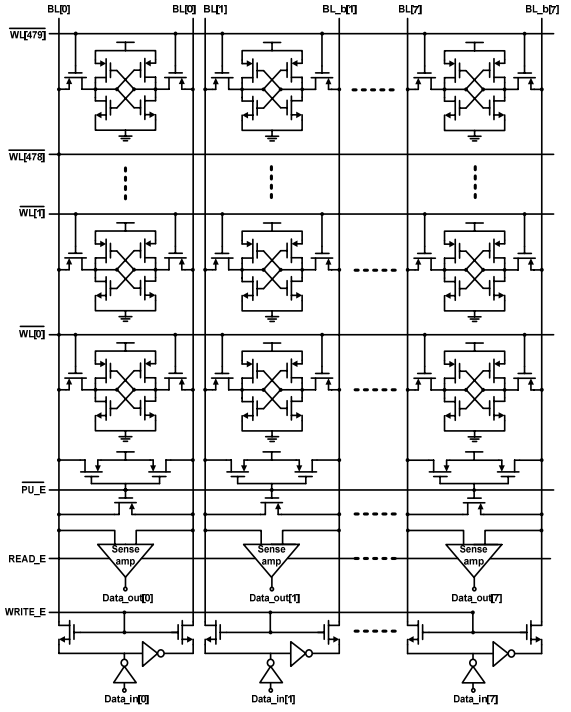


Fig. 2. Cell array of the 12k-bit SRAM

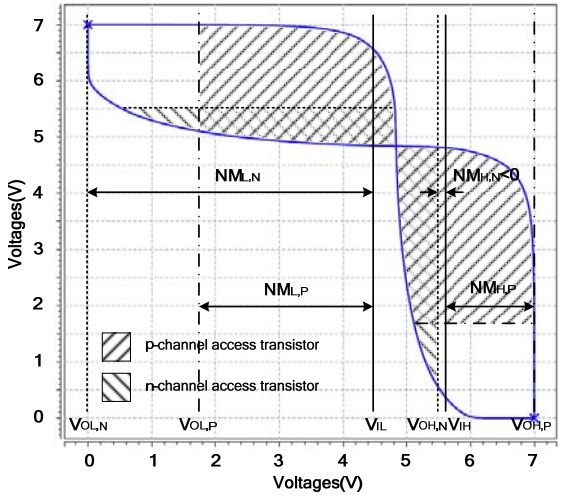


Fig. 3. Voltage transfer characteristic of SRAM cell

3. Mismatch immune sense amplifier

The small voltage or current difference between the two complementary bit lines is detected by sense amplifier to provide logic output. For the case of the voltage mode sense amplifier [9] shown in Figure 4, the sense enable signal (SE) must be asserted after the voltage difference between BL and BL_B is developed to be sufficiently larger than the input offset of the sense amplifier. Due to the grain boundaries of poly-Si substrate, however, LTPS TFT shows large variation and mismatch in its characteristics and therefore the sense amplifier in Figure 4 shows large input offset. Then, the read access time can be excessive or the read operation itself may be impossible if the offset is larger than the maximum read-out voltage difference of SRAM cell (very probable for LTPS TFT).

In this work, we have developed the mismatch immune sense amplifier shown in Figure 5. During Φ1, the bit line voltage Vbl is applied to the gate of n-channel TFT while the gate and drain of p-channel TFT is shorted together and the capacitor C2 stores logic threshold voltage of inverter. The drain currents of n-channel and p-channel TFTs are same, that is, Ip=In(Vbl) which is determined by the voltage level of Vbl. During Φ2, the complementary bit line voltage Vbl_b is connected to the gate of n-channel TFT while the gate of p-channel TFT is floating. Because the gate voltage of p-channel TFT is the same as the value sampled at Φ1, its drain current is In(Vbl) while the drain current of n-channel TFT is determined by the voltage level of Vbl_b. Therefore, the capacitor C2 is charged to VDD if Vbl > Vbl_b or discharged to GND if Vbl < Vbl_b as shown in Fig. 6-(b) and (c).

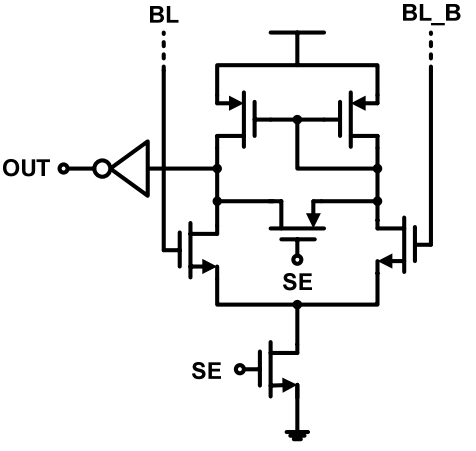


Fig. 4. Conventional voltage sense amplifier

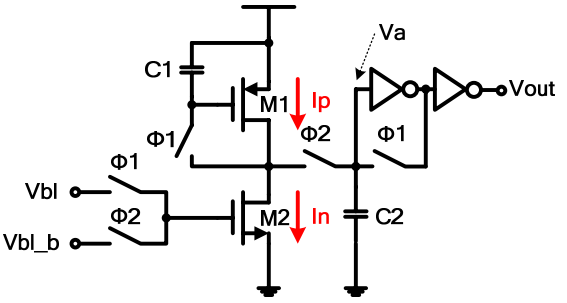
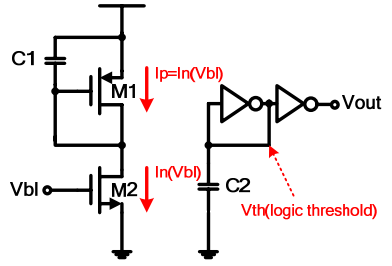
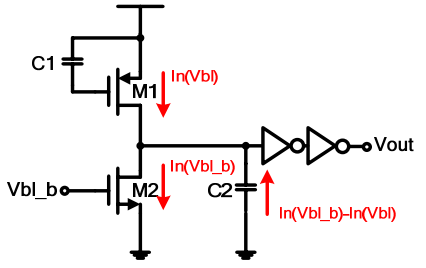


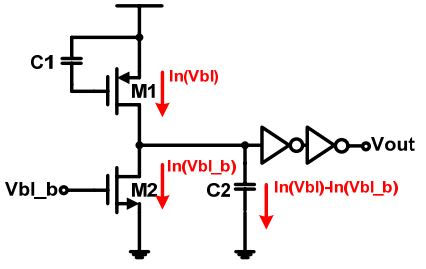
Fig. 5. Mismatch immune sense amplifier



(a) Φ1 period



(b) Φ2 period (logic LOW ; Vbl<Vbl_b)



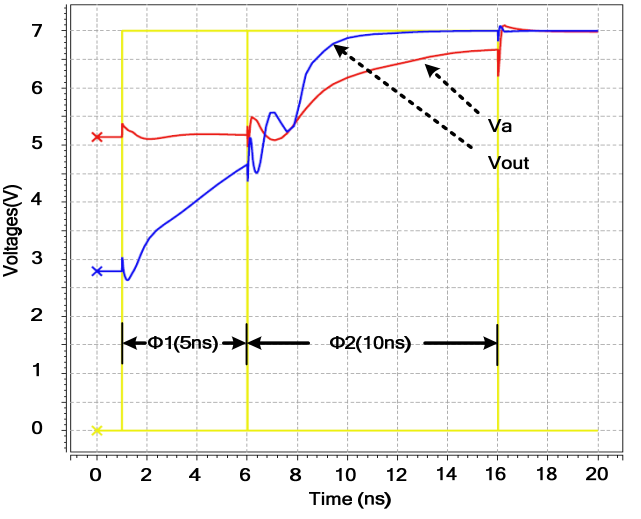
(c) Φ2 period (logic HIGH ; Vbl>Vbl_b)

Fig. 6. Sensing operation of mismatch immune sense amplifier

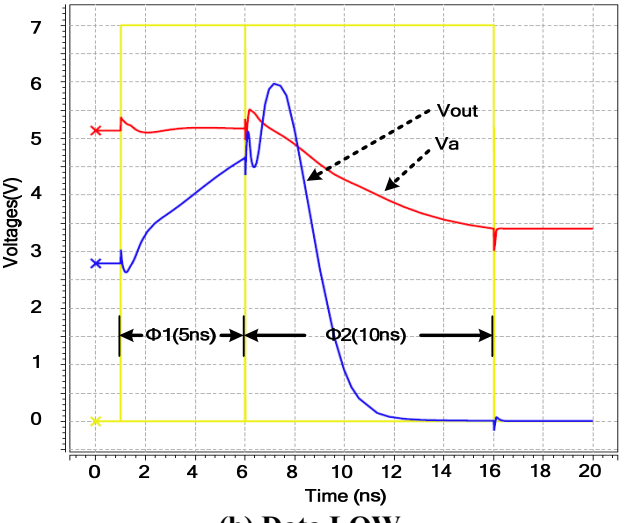
4. Simulation results

The SRAM has been developed with a 2μm LTPS TFT technology. To verify the operation of the sense amplifier, SPICE simulation of proposed sense amplifier is achieved in the condition of the worst case process variation to see the compensation results. At first, we assume that ΔV (voltage difference of Vbl and Vbl_b) is 200mV. And then suppose that the threshold voltage variation of each TFT is ±200mV and mobility variation is ±20%. At this point, the worst case of reading operation happen when the sense amplifier senses data LOW or data HIGH. In case of sensing data LOW, the worst case is when p-channel TFT has -200mV threshold voltage and +20% mobility and n-channel TFT has +200mV threshold voltage and -20% mobility. In the other case, sensing data HIGH, p-channel TFT has +200mV threshold voltage and -20% mobility and n-channel TFT has -200mV threshold voltage and +20% mobility.

For 40MHz clock operation, sensing period Φ1 is determined 5ns and Φ2 is 10ns. Figure 7 shows the simulation result of the proposed sense amplifier with worst case conditions. As the results are seen in the graph, the proposed sense amplifier can read the data in the SRAM cells fast and accurately in spite of large process variation.



(a) Data HIGH



(b) Data LOW

Fig. 7. Simulation result of proposed sense amplifier

Figure 8 shows the reading operation of SRAM. SA_out is the output voltage of sense amplifier and Data_out is the output of data I/O circuit. The control signal WL_E, PU_E and Φ1,2 are word line enable, pull-up enable and sense amplifier switching control signal, respectively. And the measured access time is 30ns.

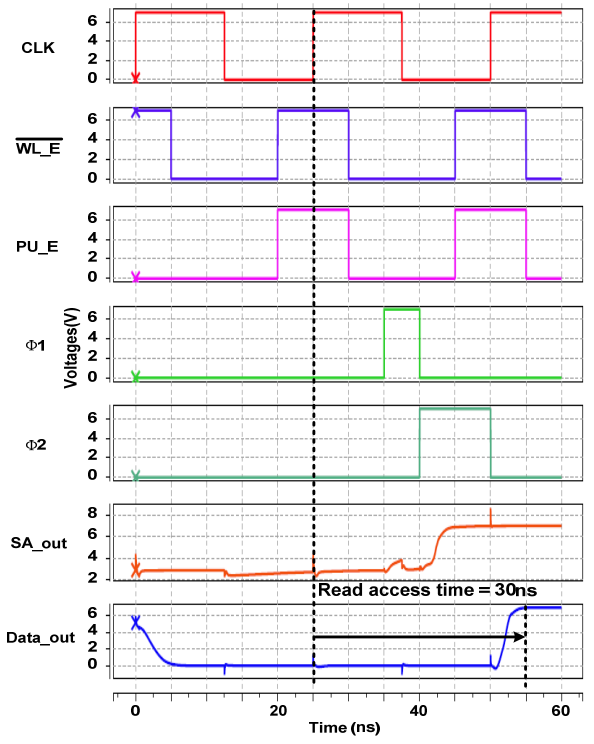


Fig. 8. Simulation result of reading operation

5. Conclusion

In the above, we introduced a LTPS TFT SRAM with mismatch immune sense amplifier. In reading operation, using proposed mismatch compensation scheme the SRAM operates fast and accurately. The simulation result of implemented 12kbit LTPS TFT SRAM shows 30ns access time in reading operation and 20MHz maximum data I/O speed with 40MHz maximum clock speed. The specification of proposed SRAM is summarized on Table 1. Because of its simplicity and compactness, proposed SRAM can be very applicable to graphic memories or frame memories as well as line memories in SoG.

TABLE 1. Performance summary of 12k-bit SRAM

Process Technology	LTPS TFT (2μm channel length)
Memory Density	12kbit
Supply Voltage	7V
Read Access Time	30ns
Clock Speed	40MHz
Power Dissipation (HLHL pattern)	4.05mW (Writing Mode) 1.75mW (Reading Mode)

6. Acknowledgement

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7. References

1. A. Hideki, S. Kenji and K. Setsuo, *NEC Technical Journal*, Vol. 1, No. 3, pp. 85-88 (2006).
2. D.-J. Kim, K.-L Lee and C. Yoo, *Journal of Information Display*, vol.5, no. 4 (2004).
3. B.-D. Choi, H. Jang, O.-K. Kwon, H.-G Kim, and M.-J Soh, *IEEE Trans. Consum. Electron.*, vol. 41, no. 1, pp. 95-104 (2000).
4. O.Ishibashi, M. Iriguchi, K. Kimura, J. Ishii, D. Sasaki, H. Imai, H. Tsuchi and H. Hayama, Dig. Tech. Papers, IEEE Int. Solid-State Cir. Conf, pp. 176-177 (2006).
5. T. Nakamura, H. Hayashi, M. Yoshida, N. Tada, M. Ishikawa, T. Motai and T. Nishibe, Dig. Tech. Papers, SID Int. Sym., pp. 1054-1055 (2005).
6. C. Yoo and K.-L. Lee, *IEEE Trans. Consum. Electron.*, Vol. 51, No 2, pp. 606-610 (2005).
7. C. Yoo, D.-J. Kim and K.-L. Lee, IEEE Electronic Letters, Vol. 41, No.2 (2005).
8. K. Min and C. Yoo, Dig. Tech. Papers, Int. Meeting on Information Display, pp. 1791-1794 (2006).
9. J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits – A Design Perspective 2nd*, Prentice Hall (2003).