Joule-heating induced crystallization (JIC) of amorphous silicon films

Won-Eui Hong[1], Joo-Yeol Lee[2], Bo-Kyung Kim[1], and Jae-Sang Ro[1,2]
[1]Department of Materials Science and Engineering, Hongik University, Seoul, 121-791, Korea
[2]EnSilTech Corporation, Seoul, 153-768, Korea
Phone :82-2-320-1698, e-mail: jsang@wow.hongik.ac.kr.

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Abstract

An electric field was applied to a conductive layer to induce Joule heating in order to carry out the crystallization of amorphous silicon. Polycrystalline silicon was produced through a solid state transformation within the range of a millisecond. Uniformly distributed grains were obtained due to enormously high heating rate.

1. Introduction

Active matrix organic light emitting diode (AMOLED) has recently come into the spotlight for its applicability to the next-generation flat panel displays. Since the device operates in a current-driven mode uniform source/drain current is critical for uniform picture quality. Low temperature polycrystalline silicon is thus preferred to a-Si for the thin-film-transistor (TFT) backplanes. A crystallization technology should produce poly-Si having a uniform grain size over the whole panel especially for AMOLED application. The methods of forming polycrystalline silicon at a low temperature include SPC [1], MIC [2], MILC [3], ELC [4], and MICC [5]. We reported a crystallization technique named as Joule heating induced crystallization (JIC) at SID '06 [6]. In this technique, Joule heat was generated by a conductive layer located beneath or above the amorphous silicon film, and was used to raise the temperature of the silicon film to crystallization temperature. For the crystallization of a-Si films to occur, the Joule heat generated must be used mainly in raising the temperature of the film to its crystallization temperature. Thus, an electric field was applied to the conductive layer for a very short time in order to generate intense pulses of energy which were conducted to the film, therefore minimizing the heating of glass substrate. As the Joule heat is generated uniformly throughout the conductive layer, the temperature of the film can be regarded as being more uniform than that achieved using other conventional heating methods. Crystallization was accomplished within the range of a millisecond by solid state transformation.

2. Experimental

Figure 1 illustrates the schematic diagrams of the JIC specimen. Figure 1(a) shows an instance in which a conductive layer is located beneath the amorphous silicon films. A conductive layer such as Mo, Cr, or ITO and a SiO_2 dielectric layer are successively formed on the dielectric layer produced on the glass substrate, which is then followed by the formation of an amorphous silicon thin film thereon. Figure 1(b) exhibits a case in

which a conductive layer is located above the amorphous silicon films. In this instance, a SiO_2 dielectric layer and a conductive layer are successively deposited on the amorphous silicon films.

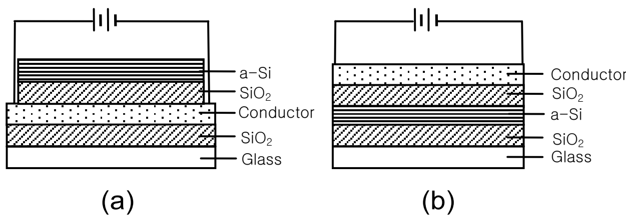


Fig. 1 Schematic diagrams illustrating the constitution of a JIC specimen (a) A conductive layer is located beneath the amorphous silicon films. (b) A conductive layer is located above the amorphous silicon films.

Using the plasma enhanced chemical vapor deposition (PECVD) method, a SiO_2 layer (first dielectric layer) with a thickness of 300 nm was formed on a 0.7 mm-thick glass substrate. An ITO thin film (conductive layer) having a thickness of 70 nm was deposited on the first dielectric layer by sputtering, and then a SiO_2 layer (second dielectric layer) having a thickness of 500 nm was deposited thereon using the PECVD method. The PECVD method also resulted in an amorphous silicon thin film having a thickness of 50 nm being deposited on the second dielectric layer. Thus, an array, including the amorphous silicon thin film shown in Fig. 1(a), was prepared. The sheet resistance of the conductive layer was measured to be 30 Ω/□. An electric field was applied to an ITO film within the range of a millisecond for crystallization. The microstructure of crystallized films was determined by transmission electron microscopy (TEM). Ion shower doping followed by activation annealing was conducted to check the macroscopic uniformity of crystallinity by measuring the sheet resistance of the crystallized silicon films over the whole crystallized area.

3. Results and discussion

Two main factors whether crystallization occurs or not using a JIC process are power density and pulsing time. When an electric field was applied with the power density of 40800 W/cm^2 for 30 μs, crystallization was not observed to occur. The 100 μs pulse with the power density of 22120 W/cm^2 resulted in partial crystallization. Meanwhile, complete crystallization was observed with the power density of 9800 W/cm^2 for 500 μs. Figure 2 indicates the simulated temperature profile under these three different processing conditions. As the power density increases the heating rate increases as shown in Fig. 2. Joule heating under each three condition causes the temperature of the film to rise above 1400 K. However, the duration above a critical temperature during the period of heating and cooling should affect the crystallization kinetics.

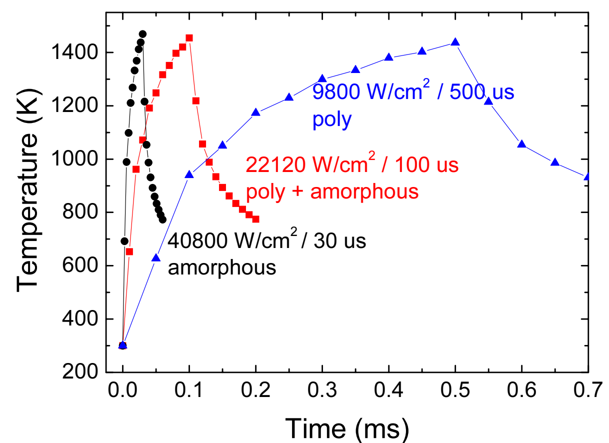


Fig. 2 The simulated temperature profile according to the processing conditions such as the power density and the pulsing time

In order to investigate the temperature dependence of the crystallization kinetics, we conducted SPC experiments using silicon wafers that had the structure of a 50 nm-thick a-Si / 500 nm-thick SiO_2 / silicon wafer. While the crystallization process was completed in 20 hrs at 600 °C, it was over in 25 sec at 1000 °C. Since SPC kinetics is controlled by the nucleation rate, and the activation energy needed to nucleate silicon crystals has a high value of 3.9 eV [7], the crystallization rate is dramatically increased when the crystallization temperature is raised. Moreover, in the case of furnace annealing, the sample was found to be unable to reach the setting temperature of 1000 °C within 25 sec. Figure 3 indicates an Arrhenius plot of an incubation time. The dotted line represents the measured data while the solid straight line denotes the estimated data using the nucleation activation energy of 3.9 eV with the measured data under 650 °C. The measured and estimated incubation time are summarized in Table 1 at crystallization temperatures ranging from 600 °C to 1300 °C. It can be seen that the incubation time indeed becomes less than 1 msec at temperatures above 1000 °C. As indicated in Fig. 3 the incubation time at 1400 K is estimated to be around 36 μs, which may explain the experimental results as shown in Fig. 2.

Figure 4 shows a TEM bright field micrograph and the transmission electron diffraction (TED) pattern of the JIC poly-Si. The a-Si film is fully crystallized at room temperature in an electric field of 800 V/cm for 0.32 msec. The radii of the TED patterns for the JIC poly-Si have been indexed and found to correspond to the interplanar spacing of silicon. The grains are preferentially oriented with the (111), (220) and (311) directions according to the TED patterns as indicated in Fig. 4(a). The microstructure of the polycrystalline silicon thin film exhibits a nano-crystalline phase. The polycrystalline silicon produced has a very small grain size of ~ 30 nm and exhibits grains of equiaxed morphology uniformly distributed in terms of the grain size. Such a microstructure cannot be obtained by solid state transformation using conventional heat-treatment methods. Crystallinity was verified by measuring sheet resistance after ion shower doping and thermal activation. The variations of the sheet resistance were observed to be within 2 %. Thus, the macroscopic uniformity of the grain size of the JIC poly-Si was found to be excellent in addition to the microscopic one.

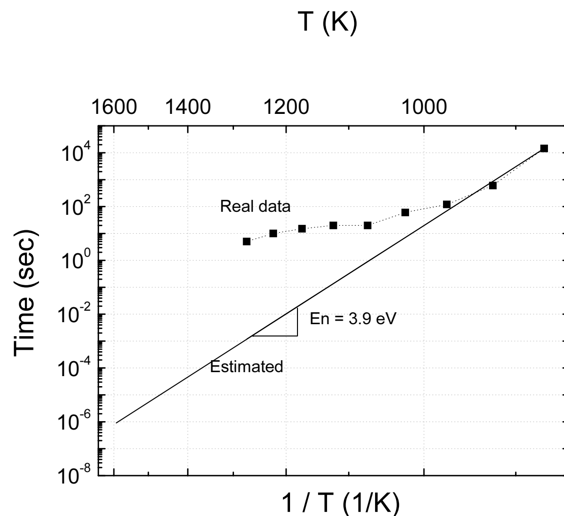
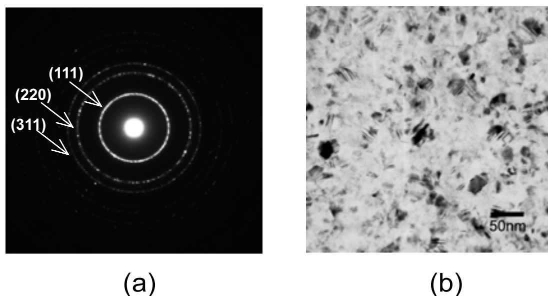


Fig. 3 Arrhenius plot of an incubation time. The dotted line corresponds to the real data and the solid line represents the estimated ones using the nucleation activation energy of 3.9 eV with the measured data under 650°C.

TABLE 1. Measured and estimated incubation time vs. crystallization temperature

	Measured incubation time	Estimated incubation time
600 ^{o}C	~ 4 hrs	4 hrs
700 ^{o}C	< 2 min	1.16 min
800 ^{o}C	< 20 sec	912 ms
900 ^{o}C	< 15 sec	25.01 ms
1000 ^{o}C	< 5 sec	1.2 ms
1050 ^{o}C	N/A	314.5 μs
1100 ^{o}C	N/A	90.5 μs
1150 ^{o}C	N/A	28.4 μs
1200 ^{o}C	N/A	9.64 μs
1250 ^{o}C	N/A	3.52 μs
1300 ^{o}C	N/A	1.37 μs



(a) (b)

Fig. 4 (a) TED pattern and (b) TEM bright-field micrograph of the JIC poly-Si crystallized at room temperature in an electric field of 800 V/cm for 0.32 msec

4. Summary

This study demonstrated the possibility of achieving the millisecond crystallization of amorphous Si thin film via Joule heating. Such a process does not make use of any metallic element for preferential nucleation, and is completed within a millisecond at room temperature. Crystallization was accomplished by solid state transformation at higher temperatures. Poly-Si film featuring nano-crystalline sized grains were obtained by the present crystallization method. As the macroscopic/microscopic uniformity of the grain size of the JIC poly-Si film is excellent, this process is expected to find its applications, especially with regards to AMOLED.

5. References

1. A.T. Voutsas and M.K. Hatalis, *J. Electrochem. Soc*, 139, 2659 (1992).
2. R.S. Wagner and W.C. Ellis, *Appl. Phys. Lett*, 4, 89 (1964).
3. S.-W. Lee and S.-K. Joo, *IEEE Electron Dev. Lett*, 17, 160 (1996).
4. J.S. Im, H.J. Kim and M.O. Thompson, *Appl. Phys. Lett*, 63, 2969 (1993)
5. Y.-J. Chang et al *SID Technical Digest,* pp1276-1279 (2006)
6. J.-S. Ro and W.-E. Hong, *SID 2006 Digest of Technical Papers*, pp1280-1283 (2006)
7. I.-W. Wu, A. Chiang, M. Fuse, L. Őveçoglu, and T. Y. Huang, *J. Apply. Phys*, 65, 4036 (1989)