

The Effects of Hydrophobic Buffer Layer Without Losing Dielectric Property on Organic Transistors

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Abstract

The buffer layer was spin-coated on the dielectric layer of OTFTs to introduce the hydrophobicity for enhancing the device performance. This functional layer contains the water-proof ingredient to reduce the surface energy and more importantly, does not harm the dielectric property of the dielectric layer. With the help of proposed hydrophobic layer, the transistor showed dramatic improvement at electrical performance which was almost 30 times higher mobility compared to the non-treated case. And on/off ratio was also guaranteed as 10^{5-6} .

1. Introduction

Over the past decade, organic thin film transistors (OTFTs) have attracted much attention for their versatile usages and remarkably progressed in their performances. To increase the performances of OTFTs, various approaches to modify the surface of dielectric layer artificially have been extensively studied, because it is a powerful and simple method to improve characteristics of organic semi-conducting layer. By controlling the surface characteristics of the dielectric, we can obtain a well-organized structure of organic semi-conducting layer which is critical to achieve the high performances of OTFTs. Many methods such as self-assembled monolayer [1, 2], plasma treatment [3], and introducing the functional buffer layer such as PMMA [4] have been investigated so far. However, these conventional techniques are not suitable for practical applications because of inevitable damages of dielectric layer during the process, complex procedure,

and particularly, the reduction of the capacitance. These effects cause the poor ordering and the reduced insulating property of the organic semi-conducting layer, which result in the decreased mobility and poor on/off current ratio of OTFTs.

In this research, we introduce the functional buffer layer to modify the surface characteristic of the dielectric layer without damaging it. We prepare the material named H1 by using an ingredient of water-proof agent. It has a high hydrophobicity which is known good to improve the characteristic of the adjacent organic semi-conducting layer. Also, it does not damage the insulating property of the dielectric layer unlike the other methods. As the thin film of H1 can be simply formed by spin-coating and be cured by low temperature process (130°C), this method is very powerful to enhance the device performance with simple process.

2. Experimental

To analyze the effect of additional buffer layer, we prepared two samples for comparison that have the same device structure as shown in Fig. 1 except the existence of H1 layer. The n-doped silicon was thermally oxidized to grow a 100nm thick layer of SiO₂ since it is known to exhibit a good device performance by protecting a leakage current with their fine insulating property. After cleaning the wafer via sonication in acetone and ethanol, polyvinyl alcohol (PVA) was coated as an organic insulating layer of 500nm thickness. Because PVA has a hydrophilic property and high permittivity, we

used this in our experiment. PVA was dissolved in boiling de-ionized water at 2 wt % and spin-coated in the wafer. It was baked at 120 °C for 30min. Then, the 0.1nm thick H1 buffer layer was coated. H1 has a ingredient from commercial water-proof agent. The H1 solution was mixed acetone 5wt% for spin coating and it was baked at 120 °C for 30min.

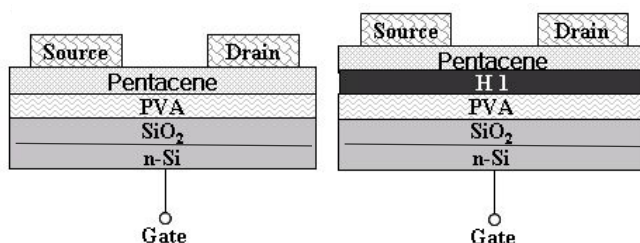


Figure 1. Device structures for comparing the effects of the buffer layer. The left figure represents the normal case while the right figure is the H1 added case.

Pentacene layer and gold electrode were sequentially deposited on both samples, in order to measure the electrical properties of the OTFTs. Pentacene was chosen for this study as the organic semi-conducting layer because it has the best electrical property among organic semi-conducting materials and it has been studied most in the OTFTs. Pentacene (99% purity) was thermally evaporated at the high vacuum ambient of 6×10^{-7} Torr with 600 Å thickness, through an aligned shadow mask to prevent the unnecessary leakage path. During the deposition, the substrate temperature was room temperature and deposition rate was 0.25 Å/s. Gold which is commonly used for source and drain is patterned using a shadow mask that has channel width of 500 μm and channel length of 50 μm. It should be noted that all steps of this treatment is carried out at a low temperature (<120 °C).

3. Results and discussion

Performance of OTFTs is affected by lots of factors. Especially, properties of the gate insulator, such as the surface wetting property and dielectric characteristic, can alter the initial growth mechanism of pentacene. To verify the surface condition and the dielectric property, we measured contact angles and capacitances. Contact angles were measured by dropping de-ionized water (Figure2). The

capacitances were measured using HP4155C semiconductor parameter analyzer with Metal-Insulator-Semiconductor (MIS) structure.



Figure 2. Contact angles of de-ionized water on PVA layer (left) and H1 layer (right). H1 layer shows much bigger contact angle than PVA layer.

As the result of measurements, the contact angle was drastically increased from 40 ° to 107 ° after coating H1 on the PVA layer. This indicates that the surface of the H1 is more hydrophobic. The measured capacitance was 1.99×10^{-8} F/cm² and 1.94×10^{-8} F/cm² for PVA and H1 on the PVA layers at 1MHz, respectively. This difference of capacitances is relatively smaller than other researches [4]. Above two results show that surface states of insulators were successfully changed to hydrophobic without considerable decrease of capacitance.

In general, a small grain size of semi-conducting layer decreased the mobility of the device significantly since the grain boundaries act as trap sites in charge transport, limiting the carrier mobility. It is known that large grains of OTFTs lead small contact resistance [5].

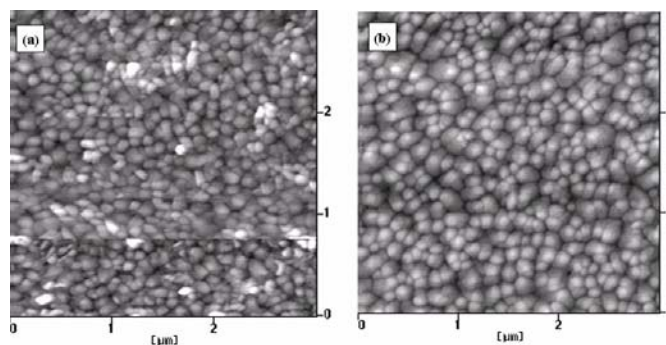


Figure 3. Microscopic images of pentacene films deposited on PVA layer (left) and H1 layer (right) observed by AFM

Figure 3 shows the surface images of pentacene layer in our experimental samples using the Atomic Force Microscopy (AFM). By analyzing the surface morphology, the relative grain size of H1 treated case is much bigger than that of normal case. The diameter of pentacene grain on H1 is about 2.5 times bigger than that of pentacene on PVA. We believed that this

well arranged structures and increased grains of pentacene molecules come from the high wetting property of the H1 buffer layer.

This can be verified by comparing the measurement of X-ray diffraction (XRD) profiles of pentacene layer. At the corresponding XRD pattern of pentacene, the case of using H1 buffer layer also showed higher peak at 5.7° (thin-film phase) than the other as depicted in Fig. 4 The enhanced peak intensity of thin film phase of pentacene on H1 represents that significant fraction of pentacene molecules were more dominantly ordered. AFM and XRD studies tell us that the initial growth mechanism of the pentacene at the interface is strongly affected by surface wetting properties of an insulator [6].

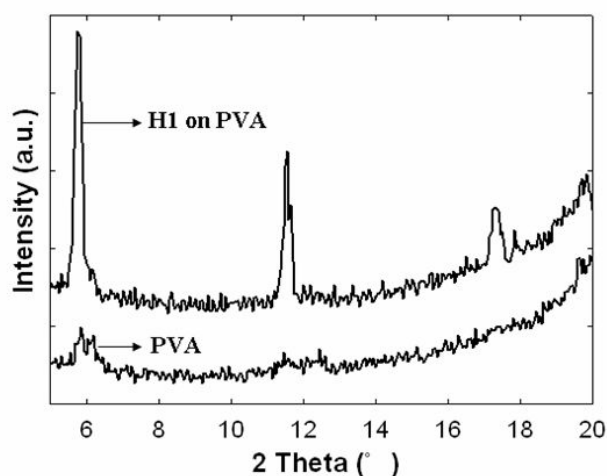


Figure 4. X-ray diffraction pattern of pentacene deposited on the PVA layer (lower) and the H1 layer (upper).

It is clear that the ordering and structural characteristics of the pentacene layer were improved by introducing the hydrophobic H1 buffer layer. Then we investigated the effects of H1 buffer layer on transistor performance. Typically, OTFT characteristics are measured at room temperature in the air immediately after the device fabrication. Figure 5 shows the electrical transfer characteristics of the OTFTs with PVA gate insulator and H1 on PVA gate insulator, where V_G was swept from +20 to -50V. The carrier mobility was extracted from the saturation regime at a drain voltage of -30V. The mobility of pentacene on PVA is $6.5 \times 10^{-3} \text{ cm}^2/\text{Vs}$ and the on/off current ratio is 10^4 . In the case of the sample with H1 coated on PVA, the carrier mobility is increased to

$0.18 \text{ cm}^2/\text{Vs}$ and the on/off ratio is also improved to 10^{5-6} .

Insulator	μ (cm^2/Vs)	Capacitance (F/cm^2)	$I_{\text{ON}}/I_{\text{OFF}}$
Without H1	6.5×10^{-3}	1.99×10^{-8}	10^4
With H1	1.8×10^{-1}	1.94×10^{-8}	10^{5-6}

Table 1. Summary for the electrical parameters

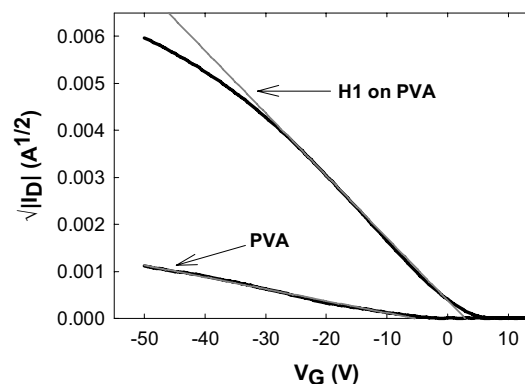


Figure 5. Electrical properties of OTFTs with only PVA insulator (lower) and, H1 buffer layer on the PVA insulator (upper). The gate voltage was swept at constant drain voltage of -30V.

The carrier mobility and $I_{\text{ON}}/I_{\text{OFF}}$ could be relatively well reproduced. The cause of the large improvement at the OTFT performance of the case of using H1 buffer layer might be the high wetting property of the buffer layer which improves the arrangement of pentacene molecules without decrease of total capacitance.

4. Summary

We investigated the performance change of OTFTs by introducing a new buffer layer (H1). Comparing with traditional methods such as self-assembled monolayer and plasma treatment, it has strong advantages of simple process, and isolation from chemical and physical damages. Also, with this method, we could maintain the good dielectric characteristic of the insulator (PVA) without changing its capacitance. In our work, the transistor showed dramatic improvement at electrical performance which was almost 30 times higher mobility compared to the non-treated case with the help of proposed hydrophobic layer. And on/off

ratio was also guaranteed as 10^{5-6} .

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6. References

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