High Speed Parallel Fault Detection Design for SRAM on Display Panel

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Abstract

SRAM cell array and peripheral circuits on display panel are designed using LTPS process. To overcome low yield of SOP, high speed parallel fault detection circuitry for memory cells is designed at local I/O lines with minimal overhead for efficient memory cell redundancy replacement. Normal read/write and parallel test read/write are simulated and verified.

1. Introduction

Recent mobile systems with display panel need small size, light weight, low power as well as high quality display image processing. SOP (System on Panel) becomes a candidate of next display panel technologies after COG (Chip on Glass) or SIP (System in Package). Recently, SOP systems have been reported in [1-3] where peripheral circuits of display panel such as CPU, audio circuits and graphic controller with 1.28Kb line buffer are integrated on a glass substrate. Inherently, display image processing needs large amount of graphic memory and several hundreds of wide I/O bit width. The data transfers between frame buffer memory and graphic controller consume large implementation area and energy, not allowed in mobile display system. Therefore, memory cells as well as interfaces with SOP are desirable. However, low yield of SOP processing technologies is main obstacle in realizing SOP memory. This paper will present SOP SRAM cells and peripheral circuits that can be used as frame buffer or line memory for display panel integration. To improve fault tolerance to alleviate low yield problem of SOP, a high speed parallel faulty memory cell detection scheme is proposed. The proposed circuits are verified with the analysis of power consumption, overhead and access times.

2. SOP memory architecture and simulation circuits

6T SRAM cell array and peripheral circuits are designed with LTPS processing technology and the performances are evaluated. It consists of 396 I/O lines (396 Sense amps and write drivers) and 25,344 SRAM cells. Fig. 1 shows hierarchical structure of the memory cell block.

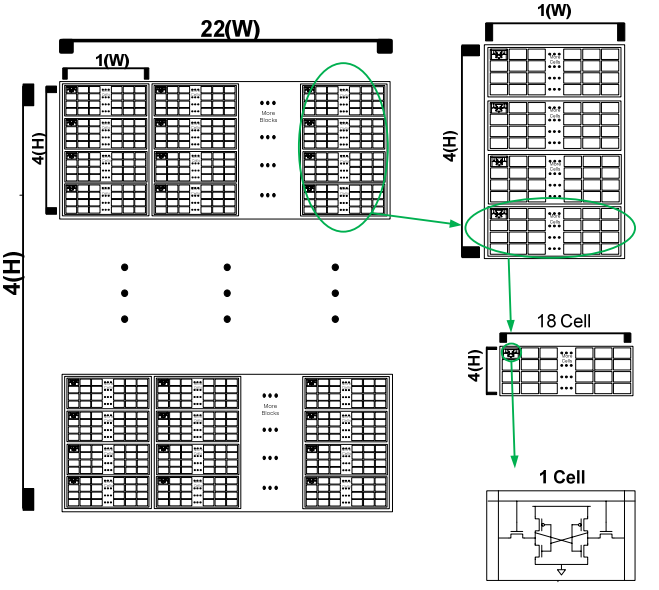

Fig. 1. SOP Memory arrays

Fig. 2 shows memory cell blocks and the peripheral circuits including write drivers, sense amplifiers and bit line conditioning circuits to optimize bit and bit bar swing during read cycle and equalization circuits to equalize I/O line pair voltage before read cycle. To reduce simulation overhead, interconnection modeling is used to replace array elements such as memory cells and bit line pairs with simpler equivalent RC interconnection models as shown in Fig. 3. The 3-segment RC model is used for accuracy. The bit line interconnection modeling is shown in Fig. 4.

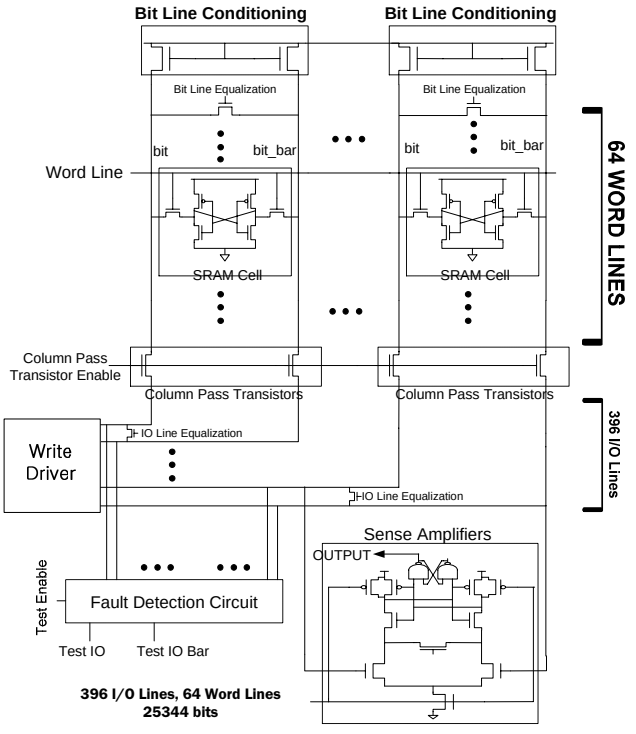

Fig. 2. Memory cell array and peripheral circuits

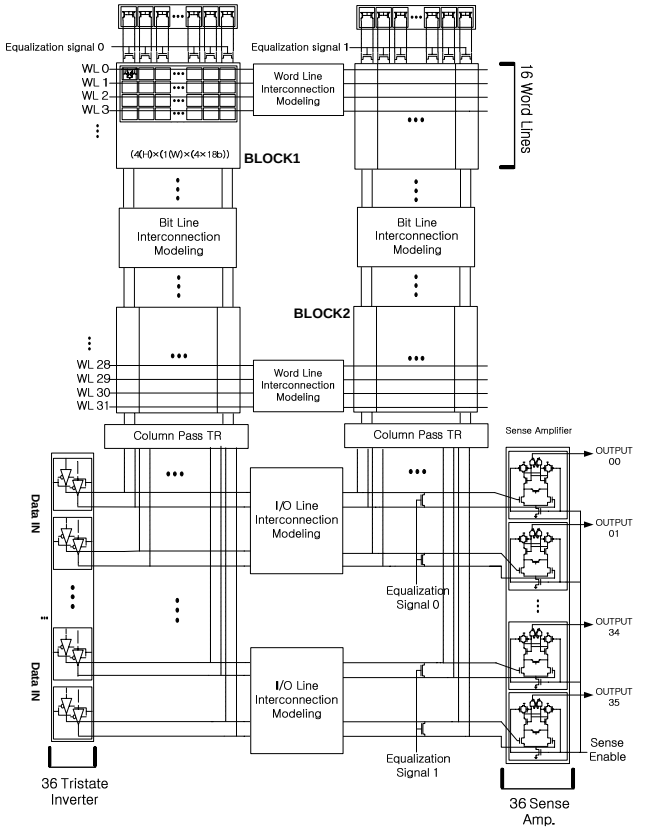

Fig. 3. Simulation Circuit

1152 of 25344 SRAM cells and 38 of 396 write drivers and sense amplifier are simulated and the rest are replaced with equivalent RC interconnection model. The worst case SRAM blocks, the left top corner (block1 in Fig. 3) and the right bottom corner (block2 in Fig. 3) are simulated because they are the farthest from the sense amps and bit line conditioning respectively.

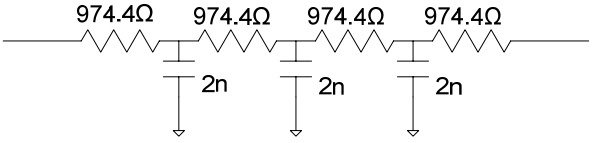

Fig. 4. Bit line interconnection modeling

3. High speed parallel faulty cell detection

To overcome low yield of SOP, redundancy memory cells are required for fault tolerance based on faulty cell detections. Therefore, hardware-efficient and fast memory cell testing is required. A high speed parallel test method is proposed in this paper to expedite the test significantly by testing a group of cells with a certain size in parallel then conducting individual cell testing only in the detected faulty group of cells. This hierarchical testing methodology saves time to locate faulty memory cells by testing all of individual cells conventionally. The principles of parallel testing are as follows. A 6T SRAM cell uses complementary input and output. The proposed parallel testing can detect the location of faulty cell groups by reading groups of memory cells in parallel after the same data are written. As shown in Fig. 5, test I/O pair generates complementary signals when the groups of memory cells being tested do not have a faulty cell. Otherwise, test I/O pair does not become complementary due to weak or faulty pull-up and pull-down transistors in a faulty memory cell.

In precharge test, bit/bit bar lines are precharged first, then memory cells with faulty pull-down transistors show weakness or incapability in pulling down during the parallel testing. These are detected by fault detection circuit as shown in Fig. 5. Fault detection circuit can be implemented with only a few transistors incurring negligible overhead compared to SRAM cell array.

In addition to the detection of pull-down and pull-up malfunction or incapability in SRAM cell, various parametric tests are realizable based on diverse test data according to activation patterns of word and bit lines. For example, by alternating bit and word line

activations, neighborhood pattern sensitive fault due to coupling can be detected.

Also, the fault detection circuit can be applied to SRAM array with hierarchical bit line and divided word line [4] as shown in Fig. 6.

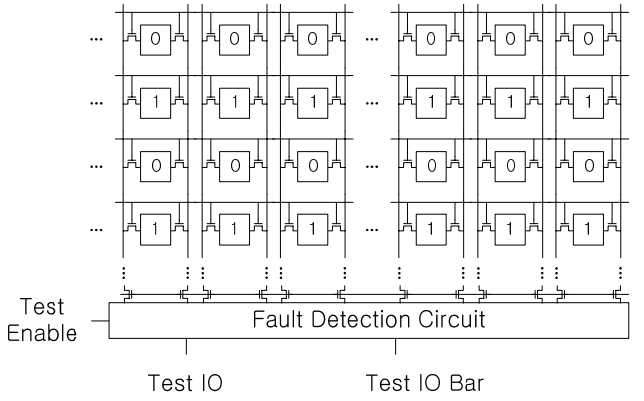

Fig. 5. Fault Detection Circuits

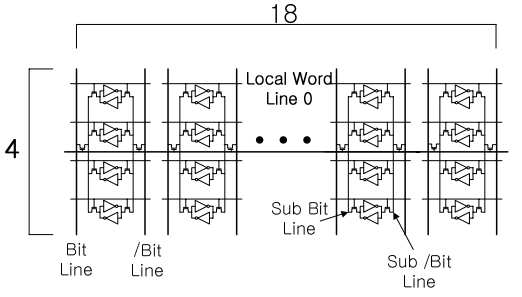

Fig. 6. Hierarchical bit line & divided word line

4. Simulation results and performance analysis

Fig. 7 and Fig. 8 show the simulation results of normal read and parallel test cycle. Write access time is estimated as rise time of 10% and 90% of cell storage node. Fig. 8 shows the read cycle where I/O pairs are equalized then developed according to word line activation. The delay of half swing in the sense amplifier output is estimated as read access time.

Fig. 9 shows test I/O pair for precharge test. The first test cycle detects a faulty cell with a faulty pull-down driver among 18 cells under test. The second test cycle shows normal case with all normal 18 cells. A separate memory cell simulation model with resistance between a driver transistor and V_{SS} is used for a faulty cell. Both test I/O pairs are pulled down, if faulty cell is detected in Fig. 9.

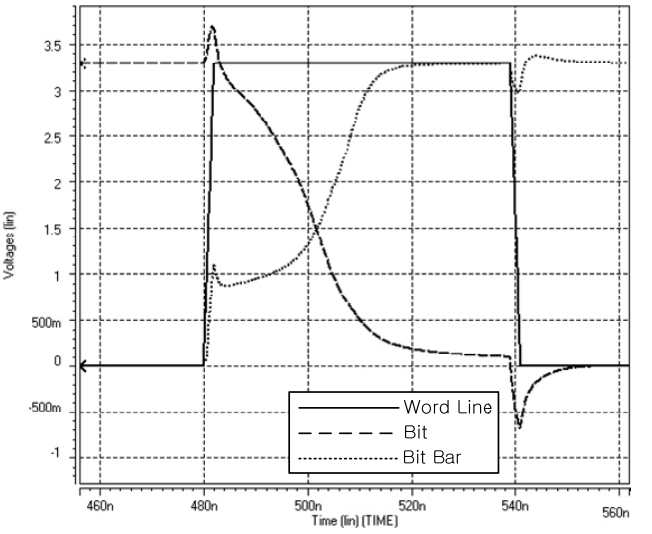

Fig. 7. Write waveform

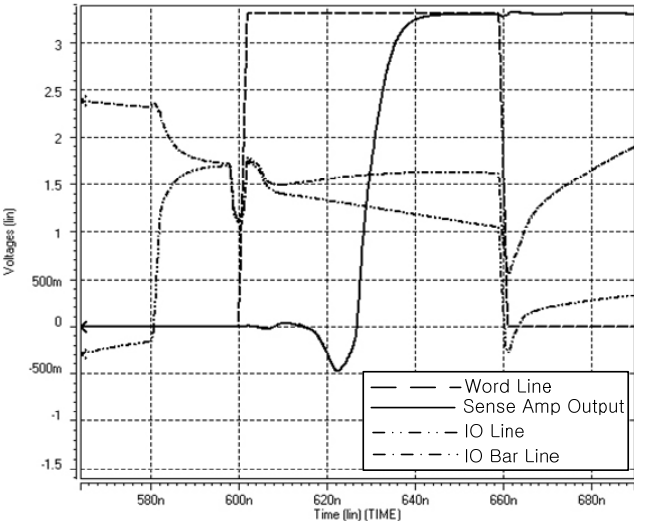

Fig. 8. Read waveform

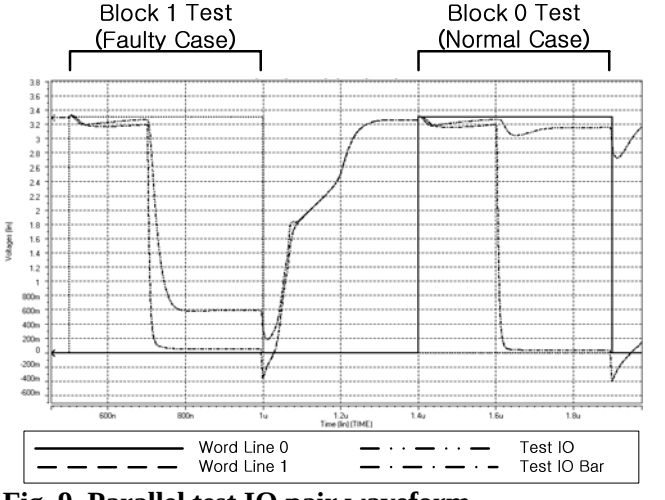

Fig. 9. Parallel test IO pair waveform

The access times of normal and parallel test read/write are summarized in Table 1. 300ns of parallel read cycle is used for enough safety margins by starting the parallel read after the voltages of bit and bit bar lines are developed sufficiently.

Table 1. Normal read/write & parallel test read/write access time

Read/write	Write	Read
Normal read/write	27ns	28ns
Parallel test read/write	27ns	300ns

Test time ratio (TTR) is defined as ratio of the time required for individual test and parallel test. Assuming one faulty cell in a memory cell block to be tested, TTR is shown in Eq. (1). In case of 64 Kbyte memory and 256 bit test group, the parallel test only takes 0.39% of the time required for individual test case. Fig. 10 shows the TTR vs. test group size and memory capacity.

$$\mathbf{TTR} = \frac{\text{Individual cell test time} \times \text{memory capacity}}{\text{Parallel test time} + \text{Individual cell test time} \times \text{Test group size}} \quad (1)$$

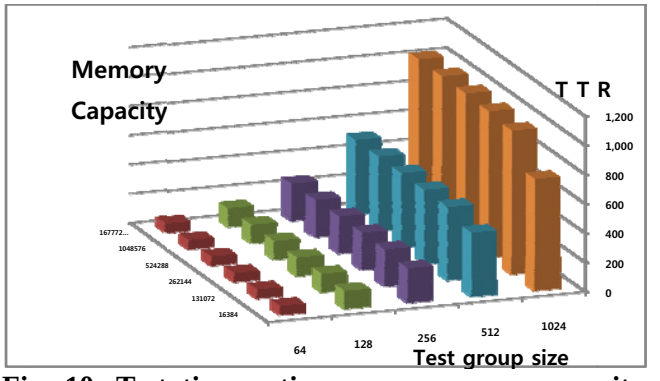

Fig. 10. Test time ratio versus memory capacity and test group size

5. Conclusion

Image memory suitable for SOP display systems is designed using LTPS process. The experimental memory is composed of 25,344 cells with 396 I/O with 28ns (27ns) access time of normal read (write) cycle. It can operate with 35MHz clock, sufficient for current mobile display systems. Furthermore, to overcome low yield of LTPS environment, a parallel faulty cell detection methodology to test group of cells in parallel based on the same written data is proposed. It facilitates tests for memory cell redundancy replacement for fault tolerance as memory cell capacity and test group size become larger as well as tests based on various memory cell test data patterns.

6. Reference

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