A High-Speed and High-Accurate Common Source Type Analog Buffer Circuit Using LTPS TFTs for TFT-LCDs

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Abstract

A high-speed and accurate analog buffer is proposed for mobile display using LTPS TFTs. The proposed analog buffer is common source type with sampling and negative feedback mode. Therefore, driving speed of the proposed buffer is faster than previously reported one. In addition, the accuracy is very high because of high negative feedback gain. The simulation results show that maximum mischarging voltage of the proposed buffer is 8mV and previously reported one is 37mV. And Power consumption of the proposed buffer is 43.1μW, which is 73% of previously reported one.

1. Introduction

Low Temperature Polycrystalline Silicon (LTPS) technology has a potential to integrate the driver circuits of TFT-based displays with pixel array because of some merits such as a high current driving capability and low cost by integrating peripheral circuits. However, LTPS TFT has some inferior electrical characteristics to single crystal Si transistor, which include high threshold voltage and non-uniformity of electrical properties.

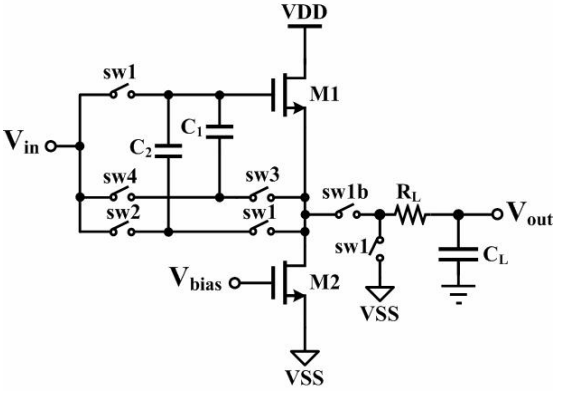


Fig. 1. Schematic diagram of previously reported analog buffer [4].

Recently, the market of mobile device has rapidly grown. The demand for more compact size, higher resolution, and higher quality images in mobile devices has grown as well. Especially, to realize high quality display, the resolution of display and output load must be increased. On the other hand, the line time need to be reduced. Thus, the capability of analog buffer should be superior in order to charge output load in a line time. However, analog buffer using LTPS TFTs has a problem to increase mischarging voltage because of poor electrical characteristics and their non-uniformities of LTPS TFTs.

In order to reduce mischarging voltage, many analog buffers such as differential type[1], comparator type[2], source follower type[3], and source follower type with double compensation[4] have been developed. But, these buffers are not suitable for high resolution display due to the following reasons.

Differential type buffer has the problem of input stage mismatching due to non-uniform electrical characteristics of poly-si TFTs and comparator type buffer consumes large amount of power because of static current during comparator operation. Generally, source follower type buffers have slow-speed operation characteristic because of the decrease in $|V_{gs}|$ as input voltage follows output voltage.

To achieve high-speed operation and high-accuracy, we proposed an analog buffer with common source type.

2. Proposed driving scheme

Figure 2 (a) shows the schematic of the proposed buffer. It consists of three capacitors, two p-type TFTs and one n-type TFT. The proposed buffer operates in three phases: one sampling mode and two negative feedback modes.

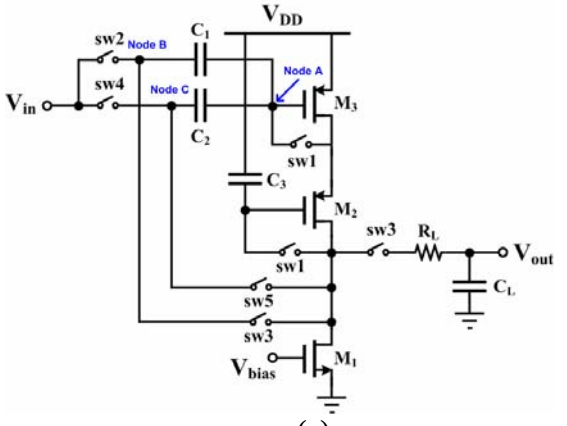
In sampling mode, as shown in figure 2 (b), SW4

and SW2 are on. Then, SW1 is on at the end of sampling phase. Thus, the voltage at node A is |VDD – V_{th}|. The voltage across capacitor (C1) and capacitor (C2) is V_{in}-|VDD - V_{th}|. This voltage across capacitors keeps up during the whole operation.

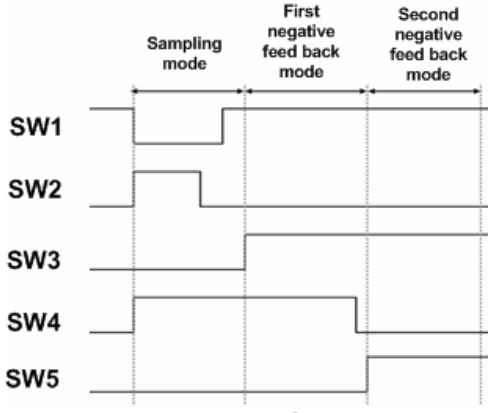
In the first negative feedback mode, SW2 is off and SW3 is on and SW1 keeps on. At the beginning of the first negative feedback mode, the current of M3 transistor has $g_m \cdot |VDD-V_{th}|$. While the output voltage increases, the voltage at node B also increases. As a result, the voltage at node A increases until the output voltage equals the input voltage.

To increase accuracy, SW5 is on and the circuit enters the second negative feedback mode.

M2 P-type TFT makes output-resistance high for negative feedback gain and it can reduce unwanted capacitor coupling between the gate and the drain of M3 when SW3 is connected to output load. If SW3 connected to output voltage is on without M2 TFT, sampling error will be large. Accordingly, M2 TFT increases negative feedback gain. Therefore, the output load charging capability of proposed buffer is very fast.



(a)



(b)

Fig. 2. The proposed analog buffer: (a) schematic diagram and (b) timing diagram.

3. Simulation results

We simulated the proposed buffer using LTPS process under the condition in table 1. The settling time defines the time when the output voltage reaches less than 10mV of the target voltage because 1LSB is larger than 10mV in 6-bit gray scale.

Figure 3 shows the output waveforms of the proposed analog buffer and the previous buffer. Figure 4 shows the settling time of the proposed and the previous buffers. Output voltage of the proposed buffer is totally settled in 9.2μsec while the previous buffer is settled in 24.9μsec. Therefore, the charging time of the proposed buffer is faster than the previous one by approximately 16μsec.

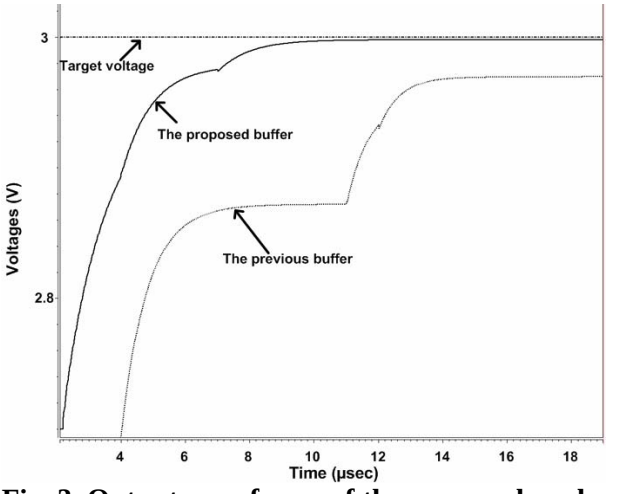


Fig. 3. Output waveforms of the proposed analog buffer and the previous buffer.

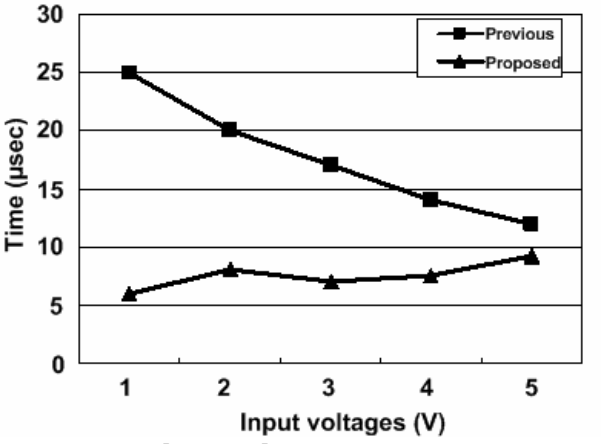


Fig. 4. The settling time comparison of previous buffer and proposed buffer.

Additionally, we compare mischarging voltages of output buffers in one third of line time of qVGA, which is 16μsec, since three sub-pixels operate in one channel source driver to reduce the height of source driver. Figure 5 shows mischarging voltage of the previous and the proposed buffer at 16μsec. The maximum mischarging voltage of the proposed buffer is 8mV and that of the previous buffer is 37mV under SS condition. Because driving capability of the proposed analog buffer is superior to the previous one, the proposed buffer charges the output load more quickly than the previous one at the target voltage during 16μsec.

Finally, the power consumption of the proposed analog buffer is 43.1μW, which is 73% of previous one. Figure 6 shows that peak current and static current of the proposed and the previous buffer. The peak current and the static current of the proposed buffer are 31μA and 2.98μA, respectively, under FF condition. Thus, the proposed buffer requires a smaller current than the previous one because the charging capability of the proposed buffer is larger than the previous buffer.

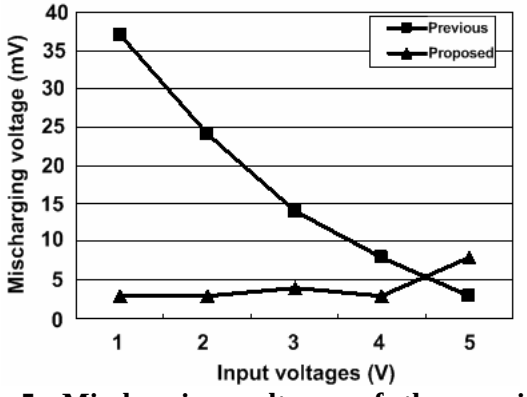


Fig. 5. Mischarging voltages of the previous buffer and the proposed buffer.

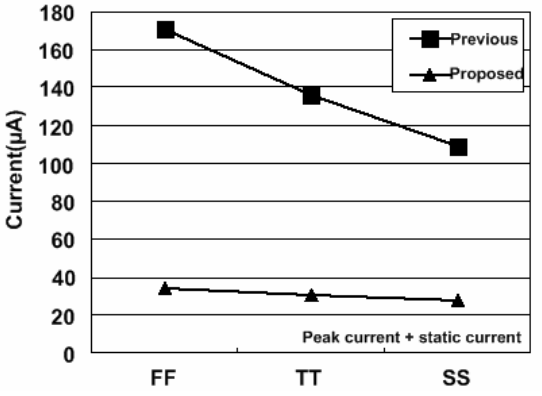


Fig. 6. The static current comparison of the previous buffer and the proposed buffer.

TABLE 1. Simulation condition

VDD, VSS	8.5V, -0.5V
Input voltage range	1V to 5V
Line time	16μsec
Load condition	C:12pF and R:900Ω

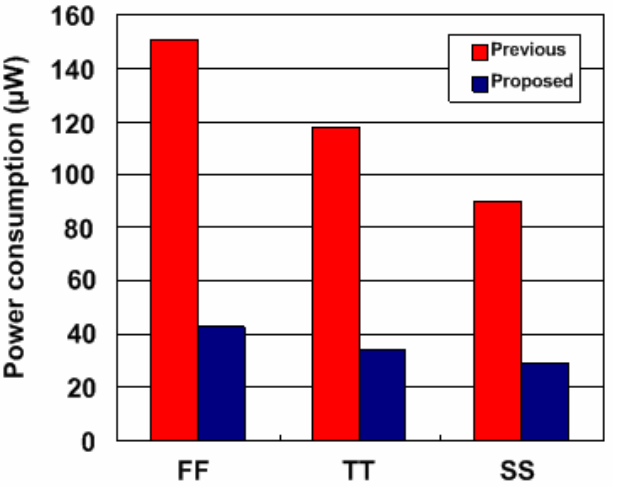


Fig. 7. Power consumption.

Therefore, it consumes less power than the previous one. Figure 7 shows power consumptions of the buffers.

4. Measured results

We fabricated the proposed buffer with common source type and measured its electrical properties under the conditions as shown in table 2. Figure 8 shows the measured output waveforms of the proposed buffer with common source type. The microphotographs of fabricated two buffers are shown in figure 9. At 16μsec, mischarging voltages of about 30mV are observed over the output voltage range because there are parasitic capacitances in the lines of test pattern glass and oscilloscope active-probe. So, it takes a delay time to charge the output load. And mischarging voltages have much higher values than the simulation results.

5. Conclusions

In this paper, a high-speed and accurate analog buffer with common source type is proposed. The settling time of the proposed buffer is about 16μsec faster than that of the previous buffer when the settling time defines the time when the output voltage reaches less than 10mV of target voltage. The mischarging voltage of output with the proposed

analog buffer is 8mV and previously reported one is 37mV. And the maximum power consumption of the proposed analog buffer is 43.1μW, which is 73% of previous one. By using this buffer, it is expected that a low power and high quality display can be realized in LTPS technique.

6. Acknowledgements

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TABLE 2. Measurement condition

VDD, VSS	10V, 0V
Input voltage range	3V to 5V
Line time	16μsec
Load condition	C:30pF

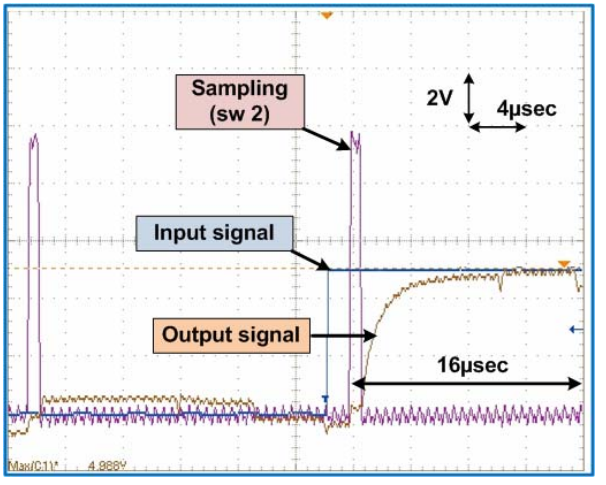

Fig. 8. Measured waveforms of the proposed buffer.

Fig. 9. Microphotograph of the proposed buffers

7. References

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