Low Power and Small Area Source Driver Using Low Temperature Poly-Si(LTPS) Thin Film Transistors(TFTs) for Mobile Displays

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Abstract

A low power and small area source driver using LTPS TFTs is proposed for mobile applications. This source driver adopts level shifter with holding latch function and new R-to-R type digital-to-analog converter (DAC). The power consumption and layout area of the proposed source driver are reduced by 23% and 25% for 16M colors and qVGA AM-OLED panel, respectively.

1. Introduction

LTPS TFTs have much better electrical characteristics than a-Si:H TFTs. So it is capable that peripheral circuits as well as pixels are integrated on the same glass substrate [1, 2]. However, high circuit-performance and uniformity of LTPS TFTs are required. Also it is necessary to design circuits considering the characteristics of LTPS TFTs. Because LTPS has a larger design rule than single crystalline silicon (c-Si), the circuit size must be increased. Also, because LTPS TFTs have wider variations of threshold voltage and field effect mobility, it is very difficult to integrate analog circuits such as output buffers [3]. Especially the power consumption and the circuit size are the most important factors in mobile display applications. So, we propose a new source driver that can realize low power consumption and small circuit area.

2. The proposed source driver

2.1 Level Shifter with Holding Latch Function

Figure 1 (a) and (b) shows the block diagram of the previously reported source driver and the block diagram of the proposed source driver, respectively. The difference between figure 1 (a) and (b) is that the proposed source driver uses level shifters with holding latch function and a new R-to-R type DAC. Especially, the proposed DAC adopts the channel resistor instead of channel R-string to reduce the number of circuit components. And the proposed source driver consumes less power and has smaller circuit area than the previously reported one.

Figure 2 shows the previously reported level shifter circuit using the cross-coupled structure and a static D-latch as a holding latch. The previously reported one consumes a large power because of short-circuit current during the transition time [4, 5].

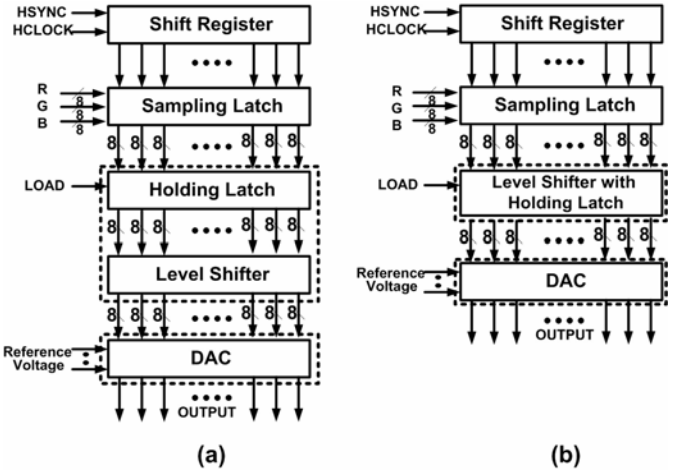

Fig. 1. Block diagram of the source driver : (a)Block diagram of the previously reported source driver and (b)Block diagram of the proposed source driver.

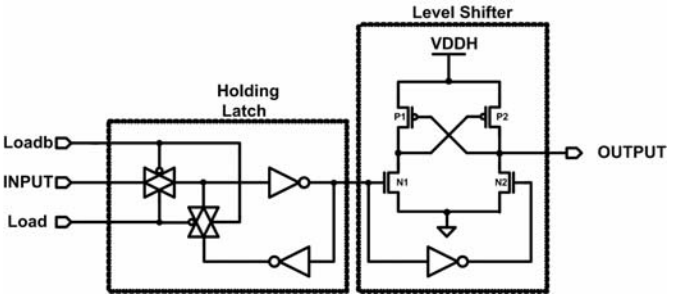

Fig. 2. Schematic diagram of the previously reported holding latch and level shifter.

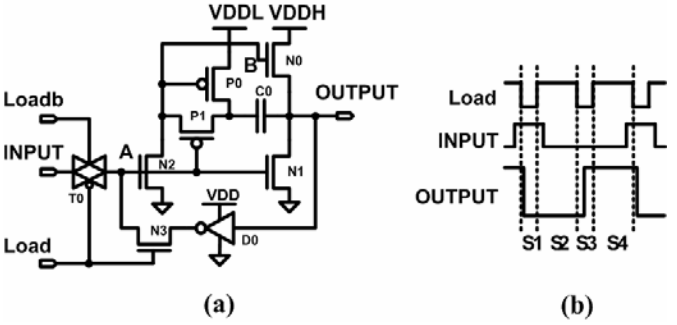

Fig. 3. The proposed level shifter with holding latch function (a)Schematic diagram and (b) Timing diagram.

Figure 3 (a) and (b) shows the schematic and timing diagram of proposed level shifter circuit with latch function, respectively. The operation of the proposed circuit is as follows.

During S1 period, the node A is high and then OUTPUT is discharged to GND and C0 is charged to VDDL. During S2 period, N3 is turned on, so the node A and OUTPUT hold their previous values. During S3 period, the node A is low and then N0 is turned on, so OUTPUT is charged to VDDH by bootstrapping at C0 and positive feedback. Then node B goes up to about VDDH+VDDL and N0 is turned on more accurately and operates more reliably and quickly. During S4 period, N3 is turned on, and the node A and OUTPUT hold their previous values.

The proposed level shifter with latch function consumes less power than the previously reported one. Also it does not have limits of the output voltage level, and the proposed one operates well reliably despite the variation of electrical characteristics of LTPS TFTs because it uses bootstrap and positive-feedback method [6].

2.2 New R-to-R type 8-bit DAC

The block diagram of the proposed new R-to-R type 8-bit DAC is illustrated in figure 4. The proposed DAC uses nine-voltage references and does not use output buffers.

The schematic diagram of the previously reported and the proposed 8-bit DAC structure are illustrated in figure 5 (a) and (b), respectively. To reduce layout size of the DAC circuit, the proposed DAC adopts switching TFTs instead of R-string.

To realize the linear 5-bit grayscale, common denominators are grouped by switches which select $SW_{1/32}$, $SW_{1/16}$, $SW_{1/8}$ and $SW_{1/4}$ as shown in figure 6, so a different R-string divider is formed according to $SW_{1/n}$. The output gray voltage is selected by switch Pn and switch Qn.

When switching TFTs using their on resistance are adopted in figure 6, the more accurate output gray voltage can be obtained because $SW_{1/n}$ serves as linear R-string. Moreover, the circuit area can be reduced considerably because the layout size of switching TFTs is smaller than R-string.

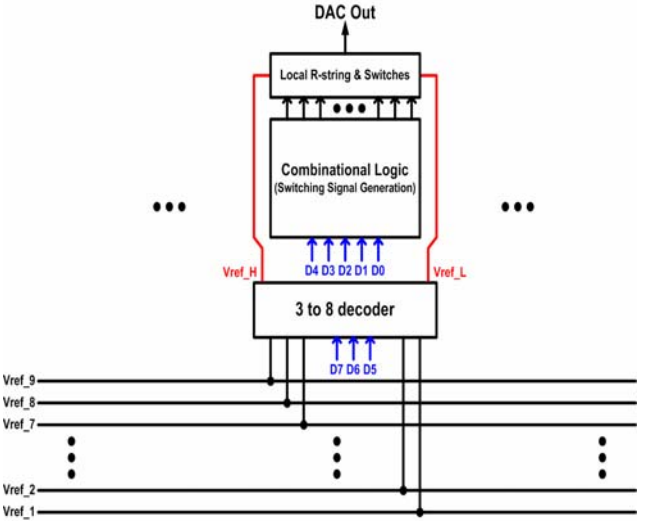

Fig. 4. Block diagram of the proposed 8-bit DAC.

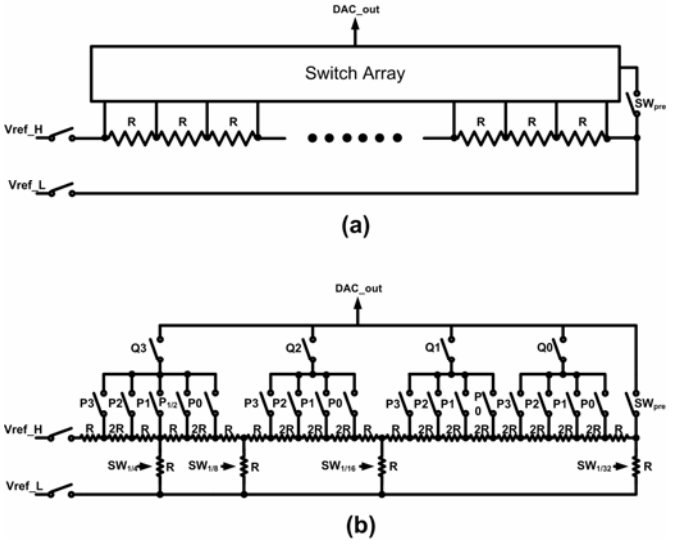

Fig. 5. Schematic diagram of channel resister DAC: (a) previously reported DAC and (b) proposed DAC.

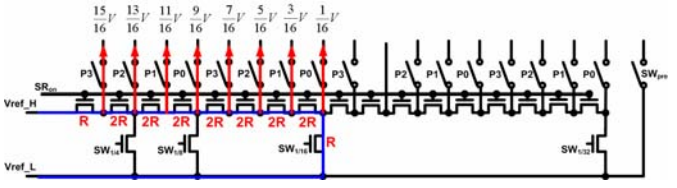

Fig. 6. Realization of 5-bit grayscale.

3. Results and discussion

Table 1 is the simulation condition of the proposed level shifter with latch function and the comparison of the power consumption for the proposed level shifter with latch function and the previously reported holding latch and level shifter. The power consumption of the proposed circuit is reduced to 77% of previously reported one.

Figure 7 shows the HSPICE simulation results of the proposed level shifter with latch function at INPUT frequency of 62.5KHz in 2.2-inch qVGA format.

The simulation condition of the proposed new R-to-R type DAC is shown in table 2. Figure 8 shows the INL and DNL of the proposed new R-to-R type DAC.

TABLE 1. Simulation condition and power consumption of level-shifter with latch function

Simulation condition	Input range	0V, 5V
	Output range	0V, 10V
	Load	50fF
	Frequency	62.5KHz (16μsec)
Power consumption	Proposed circuit	1.029mW (76.8%)
	Previously reported circuit	1.340mW (100%)

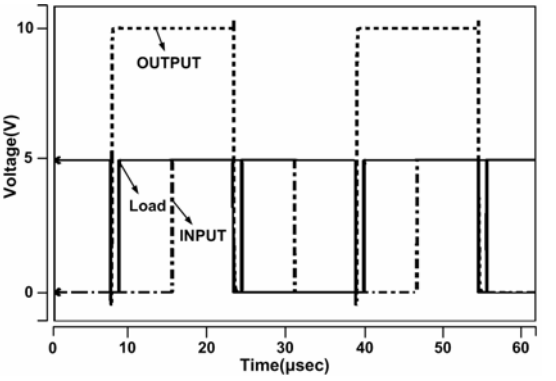

Fig. 7. Waveform of the proposed level shifter with latch function.

TABLE 2. Simulation condition of the proposed DAC

Display format	qVGA
Gray scale	8 bit
De-multiplexing	1:3
C_{load}, R_{load}	12pF, 900Ω

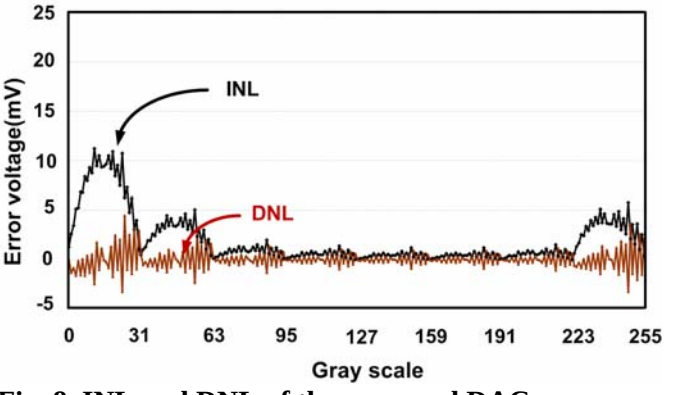

Fig. 8. INL and DNL of the proposed DAC.

As shown in figure 5, the proposed new R-to-R type DAC needs 24 switch TFTs for R-string and 22 TFTs for switch array compared to 30 resistors and 31 TFTs for switch array in the previously reported one. So it is estimated that the circuit size of proposed DAC is reduced to 24.6% of the previously reported one. So the total circuit size of the source driver is reduced considerably than that of previously reported one.

4. Conclusions

A low power and small size source driver using LTPS TFT is proposed. This source driver adopts level shifter with holding latch function and new R-to-R type digital-to-analog converter. It is verified by HSPICE simulation that the power consumption and the layout size is reduced to 23% and 25% of the previously reported one, respectively.

5. Acknowledgements

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