The Research on Vertical Block Mura in TFT-LCD

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Abstract

In this paper, a vertical block mura, which massively occurred in the LCD products, was investigated extensively by various methods, source drain (SD) line shift is found out to be one of the key reasons. This work to some extent, establishes theoretic hypothesis for further research and solutions similar issues.

1. Introduction

Mura is one type of visual defects, which shows display gray level non-uniformity on the display screen.

A simple way to detect mura is to tune the display pattern to black pattern or other low gray level pattern in the darkroom. Observing the display screen from different angles, various types of mura could be seen on the display screen along with multifarious manufacturing flaws. Vertical block mura demonstrates vertical strip pattern on the display screen, which is easy to be seen at L63 gray level, as shown in Fig. 1.

Fig.1. Vertical Block Mura

Vertical block mura occurring position, size and level are unfixed. It occurs randomly and usually appears with other defects. Vertical block mura doesn't hamper the use of display device, but it deteriorates image quality. This work attempts to solve this issue in TFT-LCD mass production.

2. Experimental

In order to find out the root cause of vertical block mura, we had carried out a series of experiments by the microscopic measurement and the theoretical calculation, which are shown as follows:

2-1).A module sample which has vertical block mura was put onto panel inspection equipment. TFT-LCD driving signal was input with Vcom voltage tuned from 3V-4.8V. The test voltages are listed in table 1. The trend of vertical block mura was observed.

Table 1.TFT-LCD Vcom voltage change test

Test Split	Vcom(V)	Test split	Vcom(V)
A	3.0	F	4.0
B	3.2	G	4.2
C	3.4	H	4.4
D	3.6	J	4.6
E	3.8	K	4.8

2-2).A module sample which has vertical block mura was used in flicker measurement.

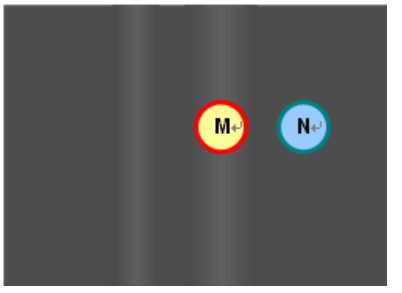


Fig.2 Normal and Vertical Block Mura area flicker measurement

The normal display area and vertical block mura area was labeled on the module. as shown in Fig. 2. The module display flicker level varied with changing Vcom voltages. The flicker-Vcom

curves were compared between the normal area and vertical block mura area.

2-3). A module sample which has vertical block mura was disassembled into panel, backlight unit and driver IC. The panel was decaped separating the TFT glass substrate from CF glass substrate. Then measure every TFT layer's Critical Dimension (CD) and overlay on the TFT Glass substrate.

3. Result and discussion

3.1

Tuning Vcom voltage from 3V to 4.8V, vertical block mura level changes consequently as shown in table 2.

Table 2.TFT-LCD Vcom voltage test result

Test split	Vcom	Vertical Block Mura leveling
A	3.0	L2
B	3.2	L2
C	3.4	L4
D	3.6	L5
E	3.8	L5
F	4.0	L3
G	4.2	L2
H	4.4	L1
J	4.6	L0
K	4.8	L0

When Vcom voltage is about 3.6-3.8V, vertical block mura becomes the worst. When Vcom voltage exceeds 4.6V, vertical block mura is very difficult to be observed. It implies that vertical block mura level is related with Vcom voltage, as demonstrated in Fig.3. Table3 is Vertical Block Mura leveling description.

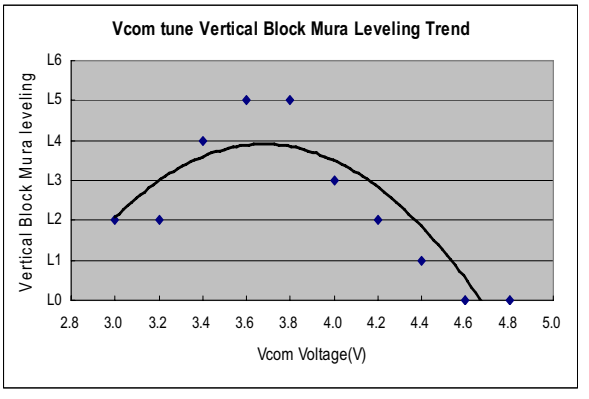


Fig.3. Vertical Block Mura level vs Vcom

Table3. Vertical Block Mura leveling description

Vertical Block Mura leveling						
weak ---------- strong ▶						
L0	L1	L2	L3	L4	L5	L6

3.2

In the flicker level measurement, the Vcom voltage corresponding to the lowest flicker level has about 0.06V difference between the vertical block mura area and normal display area, as shown in Fig 4.

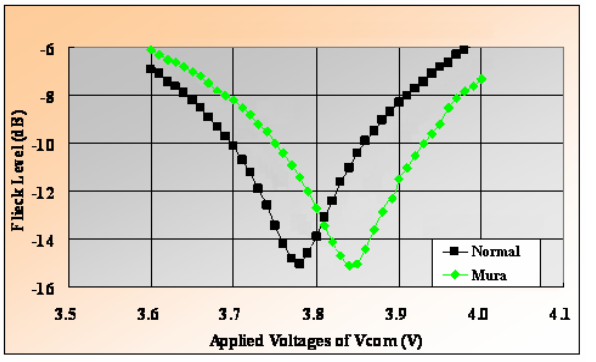


Fig 4. Flicker level curve with Vcom variation

$$\Delta Vp = dVgs + dVds$$

$$dVgs = dVg \times \frac{Cgs}{Cgs + Clc + Cst + \cdots} \quad ,$$

$$dVds = dVd \times \frac{Cds}{Cgs + Clc + Cst + \cdots}$$

Where Cgs is the parasitic capacitance between gate and source， Clc is the liquid crystal capacitance, Cst is the storage capacitance，Cpd is the parasitic capacitance between sub-pixel ITO and data line. dVg is gate line voltage range between Von and Voff，and dVd is data line signal voltage range[1].

In the above experimental result, Vcom voltage difference of 0.06V between normal area and vertical block mura area represents ΔVp difference of 0.06V. At standard L127 gray level:

$$\Delta Gray = K\Delta Vp$$

Where K is a experiential constant being 152. Δvp of 0.06V results in ΔGray of 9.12 shown in table 4.

Table 4. Vertical Block Mura flicker check result

Area	Flicker weakest Vcom (V)	Vcom warp (V)	Data Voltage (V)	ΔVp (V)	Gray warp (L127)	SD shift warp
Normal	3.78	0.06	0-11	1.72	9.12	about 0.5μm
Mura	3.84			1.66		

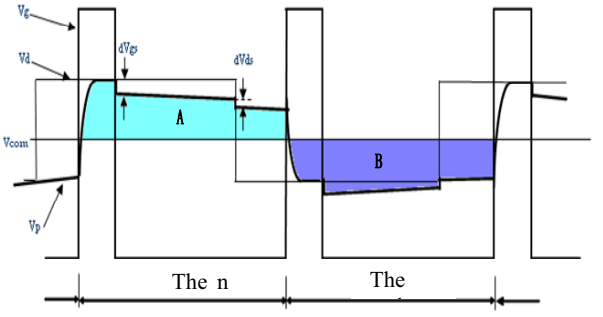


Fig.5. TFT-LCD drive

The Vcom voltage from printed circuit board (PCB) is the same for the whole panel. The difference of Vcom voltage reveals the relationship between mura and TFT load, for example expose equipment aligning system[2,3] problem in array process. Due to the coupling capacitance[4] between data line and pixel electrode, the pixel voltage changes when the data line signal changes illustrated in Fig.5.

3.3

In a pixel, there are several parasitic and coupled capacitors to affect feed through voltage (ΔVp) such as Clc, Cgs, Cpd, and Cst[5]. According to capacity calculation formula

$$C = \varepsilon\varepsilon 0 \frac{A}{d} \quad [6]$$

Know capacity relative with electrical medium, area and distance, Critical dimension and overlay on the array substrate is measured to characterize the above capacitances. According to the results shown in Fig. 6, 7, 8, SD pattern shift map has the same profile with vertical block mura. This demonstrates the relationship between SD pattern shifts and vertical block mura. Fig. 9 shows the SD pattern shift images taken under the optical microscope.

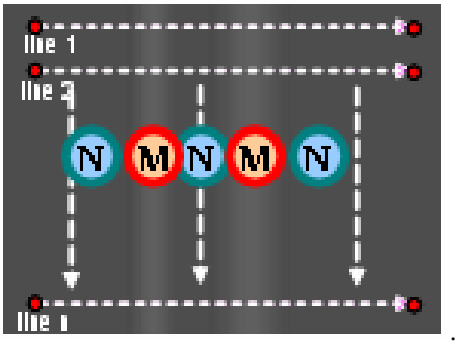


Fig 6. CD and Overlay Measure point

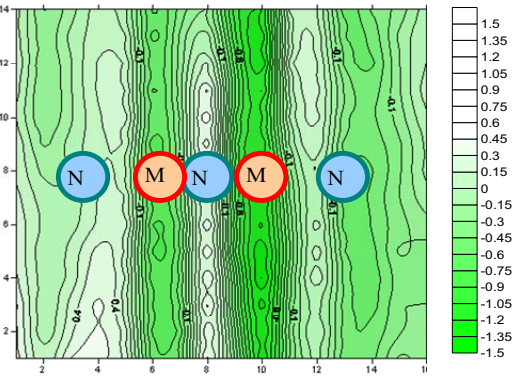


Fig 7. SD Pattern Shift Map

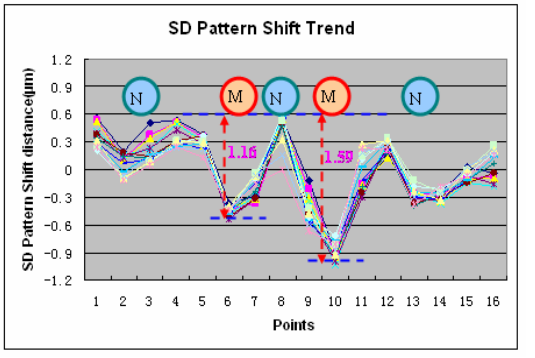
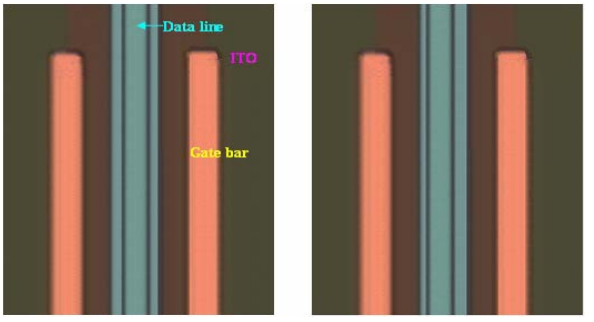


Fig 8. SD Pattern Shift Trend

According to the Table 5, SD pattern shift affects capacitance Cgs and Cpd etc, and thus affects ΔVp, luminance and gray level. Fig. 10 shows linear relationship between ΔVp and SD shift distance. When SD pattern shift exceed certain value, it results in the different coupling capacitance in the different display area. The coupling capacitance difference results in gray level difference in different display area, and vertical block mura appears.

Table5. Variable according to SD Shift

SD shift distance(μm)	-2	-1	0	1	2
Cgs(pF)	0.018	0.020	0.021	0.023	0.024
ΔVp _Cgs(V)	1.530	1.645	1.757	1.865	1.969
Cpd(pF)	0.008	0.007	0.008	0.009	0.010
ΔVp _Cpd(V)	0.104	0.101	0.103	0.114	0.133
ΔVp _Cgs+Cpd(V)	1.634	1.746	1.860	1.979	2.103
L127 luminance	111.4	83.7	63.0	45.3	37.0
Real Gray Level	158	143	127	111	97



a. Normal area pattern **b. Mura area pattern**

Fig 9. Pattern compare between normal and mura area

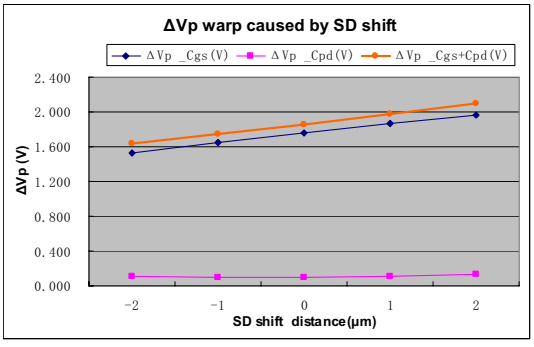


Fig.10. ΔVp trend vs SD shift

In the TFT LCD photolithography process[7], alignment offset caused by the photo mask and exposure equipments may affect the uniformity of the arc light[8]. Comparison of data pattern shift between normal area and mura area caused by the non-uniformity of exposure light[9,10] is shown in figure 9. Figure 9a is microscope picture on the normal area and figure 9b is microscope picture on the mura area. With reference to figure 9a, data line of figure 9b shifts left. The distance between data line and the left gate bar/ITO becomes smaller, while the distance between data line and the right gate bar/ITO becomes larger. This is the main reason of Vertical Block mura.

4. Conclusions

From the above experiments and discussion we conclude that SD pattern shift is one of the key reasons leading to vertical block mura. This work to some extent establishes theoretic hypothesis for further research and provides solutions to similar issues in the future.

5. Acknowledgements

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6. References

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