Pentacene Thin-Film Transistors with Polyimide/SiO_2 Dual Gate Dielectric

Hirokazu Imahara[1], Woo Yeol Kim[2], Yasuhisa Oana[2], and Yutaka Majima[1]*

[1]Dept. of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan
[2] Japan Lab., LG Philips LCD, Yokohama, Japan

E-mail: majima@pe.titech.ac.jp

Abstract

Relationships between field effect mobility and grain size on pentacene thin-film transistors with polyimide/SiO_2 gate dielectrics have been studied. 6 kinds of polyimide were used as surface treatment gate dielectric layer. Grain size of the pentacene thin film were between 5 and 30 μm and depended on the polyimide. The field effect mobility were also depended on the polyimide and the those values were from 0.027 to 0.69 $cm^2/(Vs)$. The field effect mobility tends to increase with increasing the grain size. Precursor type polyimide containing polyamic acid show better mobility of 0.69 $cm^2/(Vs)$ than soluble type polyimide. Bias stress characteristics in air are discussed in the basis of the grain size.

1. Objectives and Background

Organic thin-film transistors (OTFTs) attract a much of attention due to the relatively high field-effect mobility. In the pentacene thin-film transistors, a pentacene thin film is deposited by sublimation in which the deposition parameters can vary widely. Since the conduction channel exists at the interface between the pentacene thin-film and the SiO_2 gate dielectric, a preparation of large grain size of the pentacene thin-film is a key to obtain the high field-effect mobility. Here we introduce the polyimide films as the treatment of SiO_2 to enlarge the performance of the pentacene TFTs.

2. Results

We fabricate pentacene OTFTs with polyimide/ SiO_2 dual-gate dielectric by using 6 kinds of polyimide materials. An n^+-Si substrate used as a gate electrode, on which SiO_2 was thermally grown as a gate insulator, was subsequently spin-coated with a polyimide film (28-52 nm in thickness). Pentacene films (40 nm in thickness) as active electronic materials were uniformly formed by physical vapor deposition through a shadow mask. Then, source/drain gold electrodes were deposited by thermal evaporation through shadow mask. The channel length L was 12μm. The crystalline grain size was measured to be 5 - 30 μm using a polarized optical microscope (Figs. 1). Figures 1 show the channel current $I_D^{1/2}$ –gate voltage V_G characteristics of pentacene thin-film transistors with polyimide/SiO_2 dual gate dielectrics. Mobility on polyimide A, B, C, D, E, and F are 0.69, 0.24, 0.22, 0.13, 0.26, and 0.027 $cm^2/(Vs)$, respectively. The polyimide A (0.69 $cm^2/(Vs)$) is precursor type polyimide containing polyamic acid. The mobility was maintained under bias stress application in air for 1000 s in the polyimide A sample with large grain size of 30μm.

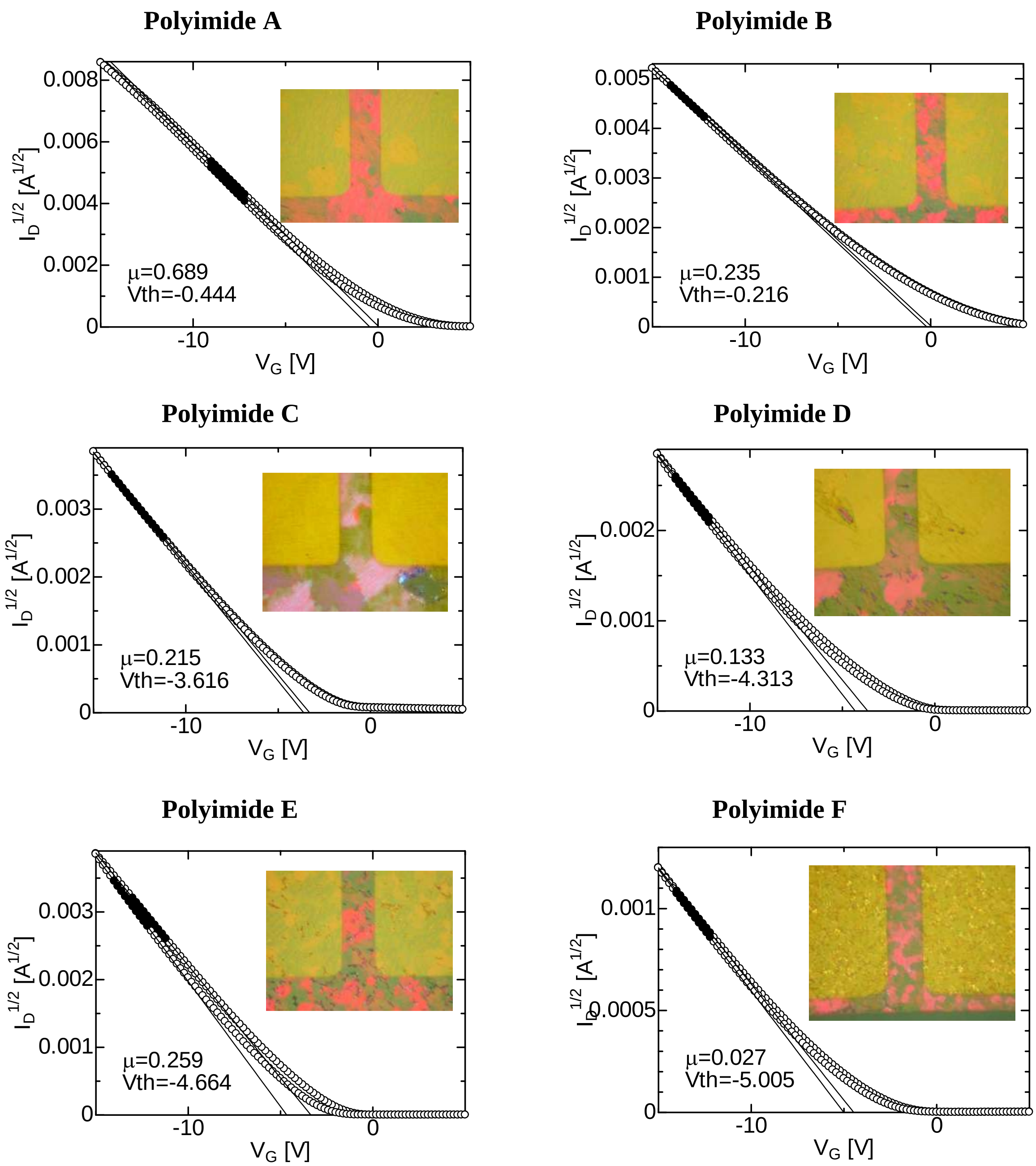
3. Impact

The polyimide/SiO_2 dual gate dielectrics give very good performances of pentacene thin-film transistors with high mobility and high stability.

References

[1] Y. Majima, D. Kawakami, S. Suzuki and Y. Yasutake, Jpn. J. Appl. Phys., 46 (2007) 390.

[2] D. Kawakami, Y. Yasutake, H. Nishizawa and Y. Majima, Jpn. J. Appl. Phys., 45 (2006) 1127.



Figs. 1. Channel current $I_D^{1/2}$ –gate voltage V_G characteristics of pentacene thin-film transistors with polyimide/SiO_2 dual gate dielectrics. Polarized optical microscope images of the pentacene TFTs are imposed in the figures. Grain sizes of pentacene on polyimide A, B, C, D, E, and F are 20-30, 5-10, 20, 10-20, 5-10, and 5, and mobility on polyimide A, B, C, D, E, and F are 0.69, 0.24, 0.22, 0.13, 0.26, and 0.027 $cm^2/(Vs)$, respectively. The polyimide A (0.69 $cm^2/(Vs)$) is precursor type polyimide containing polyamic acid.