# A Low Power Source Driver of Small Chip Area for QVGA TFT-LCD Applications

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Keywords : QVGA,LCM,EVR

#### Abstract

In this study, an architecture for 262K-color TFT-LCD source driver. In this paper proposed the chip consumes smaller area and static current which is suitable for QVGA resolutions. In the conventional structures, all of them need large number of OPAMP buffers to drive the pixels, Therefore, highly resistive R-DACs are needed to generate gamma voltages to reduce the static current. In this study, our design only used two OPAMPs and low resistance R-DACs without increasing the quiescent current. Thus, it was experted that chip would be more in consuming lower static power for longer battery lifetime. The source driver were implemented by the 3.3 V 0.35 µm CMOS technology provided by TSMC. The area of the core OPAMP circuit was about 110  $\mu$ m  $\times$  150  $\mu$ m and that of the source driver was 880  $\mu$ m  $\times$  430  $\mu$ m. As compared to the conventional structure, approximately 64.48 % in area was achieved.

## 1. Introduction

The latest mobile phone has already required millionpixel displays for mobile TV applications. The applications demand high image quality of 262k-colors and fast response liquid-crystal displays to demonstrate full grayscale motion pictures ref[4]. Especially for the motion picture, the response time is the most important parameter because of the residual image problem ref[5]. The dynamic image would become vague even for C-STN displays filled with fast response liquid crystal. Thus, more and more displays in the high-end portable production seldom tolerate the long response time, serious cross-talk and low contrast C-STN LCD and is beginning to adopt the TFT LCDs.



The cost percentage in of the driver IC the liquid crystal display module (LCM) is very high. How to redu ce the area of the driver and its current dissipation is becoming an important issue in extending the battery lifetime. However, the die size and static current are proportional to the OPAMP numbers. The OPAMP is connected as the unity-gain voltage-buffer configuration and it delivers the reference voltage to R-DAC or the grayscale voltage to the panel load. In the past, the source driver can be implemented by three architectures as shown in F ig .1. In type A architecture, it requires buffers number as the same as the output channels and its output impedance is the lowest. Thus, it possesses the largest IC die size and bias current dissipation. In type B architecture, it uses 64 OPAMPs for reference voltage buffer. However, the OPAMP requires slew rate enhancement for wide range capacitive load and no-load detector circuit to operate in 4096-colors or 512-colors mode. The no-load detector consists of three 6-input NAND gate, one 3-input NAND gate, several inverters and one RS type flip-flop to monitor RGB signals to switch the voltages buffers on/off. Thus, the equivalent die size of each individual OPAMP grows up. In type C architecture, the number of OPAMP are N, which are located in the front of the resistor for settling the 64 gamma voltages and its output impedance is the highest. Hence, the string resistor of DAC can't have low resistance value for dividing gamma voltage. The number of N is eight and they are often located at  $V_{r0}$ ,  $V_{r1}$ ,  $V_{r8}$ ,  $V_{r20}$ ,  $V_{r43}$ ,

 $V_{r55}$ ,  $V_{r62}$  and  $V_{\gamma 63}$ , which resulting from the T-V curve of the liquid crystal is not linearity.

Although above type B and C architectures can reduce the number of OPAMP to decrease the chip area and static current, but they still need the larger resistance value of R-DAC for dividing gamma voltages in normal operating or require additional power switches to reduce the current consumption during the partial-colors mode. However, the larger resistance string resistors or power switches also need more die size. This paper presents one availably architecture of the TFT-LCD source driver with two very common OPAMPs and small R-DAC for QCIF+ resolution panel. The following features are the advantages in this source driver architecture. The OPAMP circuit is one of very common architectures without slew-rate enhancement or additional control circuit. The R-DAC of gamma voltage generator occupies small die dimension. Total quiescent current dissipation is ultra low. And it don't use no-load detector or additional power switches in partial-colors mode.

#### 2. Experimental

The OPAMP、R-DAC and decoder have the larger size in the driver. For reducing chip size, the decoder can use a smaller decoder, and decrease the number of OPAMPs or d e-crease the resistance of the R-DAC. In type A, per output using one OPAMP, one driver has 528 buffers on a 240 RGB×320 resolution panel. Type B uses 64 OPAMPs for stable gamma voltages of 64 levels and type C only uses several OPAMPs for reference voltages in the front of gamma voltage generator [1][2]. All above three types of source drivers require high resistance value of R-DAC often in mega ohm class to hold the lowest static current. But, in this type D architecture, the source driver only uses 2 OPAMPs for buffers and small value of gamma resistor, as illustrate in Fig. 2.

During urging the chip to operate, control Shift Register with STP when at the beginning, show panel RGB that input materials deposit in Sample Register. Utilize, Decoder at this moment collocate POL signal change corresponding voltage of simulation and output several materials of Latch from OUT1 to OUTb in TFT-LCD panel.

Observing the signal the middle Latch can find the si gnal of locking that DFF inside does not need more complic ated function to only need to store only, so we change sever al circuit change into simpler DFF not only the all right fun ction has not been influenced, can also reduce 40% of the ar ea.

Another advantage is the elimination of the output deviatio n issue occurring in the OPAMP. In type A, resulting from p er driver output needing one OPAMP buffer, thus the output deviation is the most serious, even using the offset canceli

ng technology to eliminate the deviation issue. Type B and C can use several electronic volume registers (EVR) to fine tune 64 gamma voltages for solving this deviation problem. In type D, it just needs to adjust the two rail input gamma voltages.

By forerunner to bring up that, in order to achieve the higher power conversion efficiency and the larger current driving capability, the push-pull amplifier of class-B configuration is used for the output buffer. Its circuit is shown in Fig3. The  $M_1$  to  $M_4$  form the differential pair of rail-to-rail input, and  $M_5$  to  $M_8$  compose the cascade stage,  $M_9$  and  $M_{10}$  make up the output stage and the current source,  $I_{SOURCE}$ , equals the current sink,  $I_{SINK}$ , in this schematic. It unlikes the OPAMP in type B

source driver which must drive wide variable capacitive load. These two OPAMPs always drive the fixed panel loading during normal operation or partial-colors mode. Thus, they neither need the slew-rate enhancement circuit as driving the pixel, and nor require the no-load detector to stable the source driver or additional power switches for unused buffers as it working in the partial-colors mode. For determining the driving ability of this OPAMP, the TFT-LCD panel can be simply regarded as capacitance load.

The TFT-LCD panel can be simply regarded as capacitance load. The loading of each source driver output is about 30pF; therefore, the OPAMP has to drive more than 15840pF of equivalent capacitance within 30us settling time in type D. Conventional miller compensation requires largely area for implementing the capacitors or resistors. For saving chip size, the OPAMP can use resistive and capacitive loading of the panel to compensate the phase margin [1]. Here, the output impedance of this OPAMP is very small, thus, the resistance value of the string resistor is relatively small in R-DAC. The frequency compensation does not use the conventional Miller compensation for reducing the die size of OPAMP in this source driver. The on-chip capacitor will waste large wafer space. Here, the external loading which locates at the output terminal forms one very small dominant pole to achieve phase compensation by pole splitting in frequency response.



The 262k-colors can be mixed by the three primary colors of 64 gray-scales. Therefore, the 6 bit digital signals of each RGB display data are sent to this source driver for generating gray voltages of 64 scales. When the power supply is applied to this source driver, the reset signal, RES, will set all internal registers in the same values to avoid all channels output with different scale voltages.

It will make the TFT-LCD panel with normal white configuration to show one whole black pattern during the reset time. Then, the start pulse signal, STP, is loaded into the shift register on the rising edge of clock, CLK, and the shift register enables the correct 6 bit image data to be saved into sample register on the rising edge of following CLK. In the conventional circuit, every channel requires one shift register to enable the data register. Here, the data interface, RGB, is 18 bit bus, therefore, our source driver can work at three channels on one shift register. The CLK frequency becomes one-third of the conventional architecture and does not dissipate more area for the additional two shift registers. Since all sample registers have loaded the display data of one scanning line, the latch pulse signal, LP, will enable all latches to load display data from the sample register at one time. Then, the 6 bits decoder will output the analog gray-scale voltage to panel, depending on the polarity control signal, POL, and input 6 bit digital display data.

According to the Kudo's experimental measurement, the power dissipation of the TFT-LCD is proportional to the inversion times per frame. Therefore, the N-line inversion is the required function for trade-off the panel quality and power dissipation. In general application, the inversion period over 10 lines is one of the better settings under different frame rate and panel loading. In our proposed architecture, setting the period of the POL signal, these source driver outputs can be also operated in three different polarity inversion modes-line inversion, N-line inversion or frame inversion.

# 3. Results and discussion

The proposed architecture for 262K-color source drivers were fabricated by 3.3V 0.35µm CMOS technology. The dimension of OPAMP was 110µm×150µm. Fig.4 shows the chip layout of this source driver .The core area was 880µm×430µm.



Fig.4 The whole layout of the proposed

The Fig.5 to Fig.7 simulation drawing is a output which drives the chip, for supplying voltage (VDD =3.3v) ,Temperature (-30~80 $^{\circ}$ C) change. And real quantity examines the wave form as fig8 shows that.



Fig. 5 when VDD=3. 3v, T=80°C, Corner=FF output.



Fig. 6 when VDD=3. 3v, T=-30°C, Corner=SS output.

14

CH1 500mV



CH1 None

100mV

CH1 /

90.2696Hz



M 1.00ms

Fig. 8 real quantity examines the wave

4. Summary

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QVGA resolution panel.

X + OITTODOINNON Panon				
	this wo rk	Lu's W ork [3]	Kudo's Work [2]	Itakura's Work [1]
Fabrication Proces s	0.35μ m	0.35μ m	0.35µm	0.6µm
Power Supply	3.3v	3.3v	3.3v	5v
Output Channels	6	6	528	402
Whole Chip Size	1.9 mm <sup>2</sup>	NA	56.5 mm <sup>2</sup>	42.5 mm <sup>2</sup>
Per Unit Channel Area	$\begin{array}{c} 40625\mu\\ m^2 \end{array}$	$\frac{88800\mu}{m^2}$	$\begin{array}{c}107007\mu\\m^2\end{array}$	108508µm <sup>2</sup>
Total Quiescent C u-rrent	14.1µA	NA	NA	529μΑ

Table 1.with A high-speed low-power rail-to-rail column driver for AMLCD application comparison sheet

The authors would like to thank CIC for chip fabrication. And the research was supported in part by the Nation Science Council, Taiwan, China, under contract No.NSC-94-2218-E-005-010.

## **5. References**

[1]Tetsuro Itakura, Hironori Minamizaki, Tetsuya Saito and Tadashi Kuroda, "A 402-output TFT-LCD driver IC with power control based on the number of colors selected," IEEE Journal of Solid-State Circuits, Volume 38, Issue3, March 2003, Page(s):503–510.

[2] Y. Kudo, A. Akai, T.Furuhashi, T. Matsudo, Y. Yokota, "Low-power and High-integration Driver IC for Smallsized TFT-LCDs," SID 03 Digest, 2003, pp. 1244–1247.

[3] Chih-Wen Lu and Kuo-Jen, "A high-speed low-power rail-to-rail column driver for AMLCD application," IEEE Journal of Solid-State Circuits, Volume 39, Issue 8, Nov. 2004, Page(s):1313 – 1320.

[4] Y. Kudo, A. Akai, T.Furuhashi, T. Matsudo, Y. Yokota, "Low-power and High-integration Driver IC for Small- sized TFT-LCDs," SID 2003 Digest, 2003, Page(s):1244–1247.5. K. D. Hong, IMID'06 Technical Digest, p.877 (2006).

[5] Chih-Wen Lu and Kuo-Jen, "A high-speed lowpower rail-to-rail column driver for AMLCD application," IEEE Journal of Solid- State Circuits, Volume 39, Issue 8, Nov. 2004, Page(s):1313 – 1320.