A New-Half Bridge Converter

without DC offset of magnetizing current

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Abstract

A new half bridge converter without DC offset of magnetizing current is proposed. The proposed half bridge converter can realize no DC offset of magnetizing current as well as no circulating current, and guarantee ZVS operation. Therefore it has high efficiency and high power density, especially in wide input range. The operational principle, DC conversion ratio and ZVS analysis are presented. Experimental results demonstrate that the proposed converter can achieve a significant improvement in the efficiency

1. Introduction

Half bridge topology are well known and widely used in medium power application. In a conventional PWM half bridge converter with symmetric duty cycle, there is no dc offset current of magnetizing inductor. But it can not guarantee ZVS of all switches. To overcome this drawback, PWM half bridge converter with asymmetric duty cycle is proposed. ZVS of all switches is guaranteed by load current and magnetizing current. But it has DC offset of magnetizing current according to duty ratio. DC offset of magnetizing current induces the high conduction loss in primary side of the transformer and interrupts ZVS operation of switches. Recently, DCS(duty cycle shift) PWM half bridge converters were proposed[1][2]. DCS PWM [1] half bridge has no DC offset of Lm current but it guarantees ZVS operation of only one switch. Therefore it still has high switching loss. In DCS PWM [2], it has no DC offset of Lm current and guarantees ZVS operation of all switches. But it has high conduction loss by circulating current. To overcome these drawbacks, a new half bridge converter is proposed. Proposed converter has no dc offset current of L_m, no circulating current, and guarantees ZVS operation of switches. Therefore it has high efficiency and high power density. The operational principles, analysis and experimental results are presented to confirm the validity of the proposed converter.

2. Operation Principle

Fig. 1 shows the circuit diagram of the proposed converter. The circuit configuration of the proposed converter is similar to conventional half bridge converter except M3. Fig. 2 shows the key waveforms of the proposed converter in steady state. Each switching period is subdivided into ten modes and their topological stages are shown in Fig 3. For the convenience of the analysis of the steady state operation, several assumptions are made as follows:

(a) All parasitic components except for the leakage inductor are neglected,

(b) M1, M2 and M3 are ideal expect for output capacitor $C_{oss1}=C_{oss2}= C_{oss3}=C_{oss}$ and internal diode,

(b) The blocking capacitors C_b and output capacitor C_o are large enough to be considered as a constant voltage source DV_{in} and V_o, respectively.

(d) The transformer magnetizing current $i_{Lm}(t)$ is assumed to be constant during the time intervals t_1~t_2 and t_5~t_6.

(e) Turn ratio of transformer is n=N1/N2.

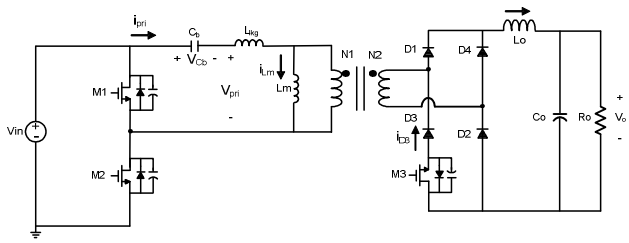

Fig. 1 Proposed Half Bridge Converter

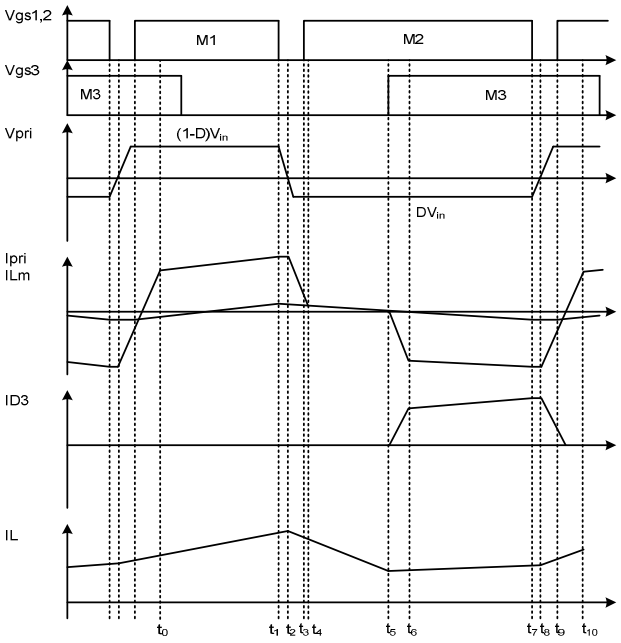

Fig. 2 Key Waveforms of the Proposed Converter

Mode 1(t_0~ t_1) : Mode 1 begins when the commutation of secondary diode current is completed. Then D3,D4 are turned off and D1,D2 are turned on, respectively. Since M1 is on state and M2 is off state, V_{Cb} is applied to L_m+L_{lkg}. The current flowing through L_m and L_{lkg} can be expressed as follows:

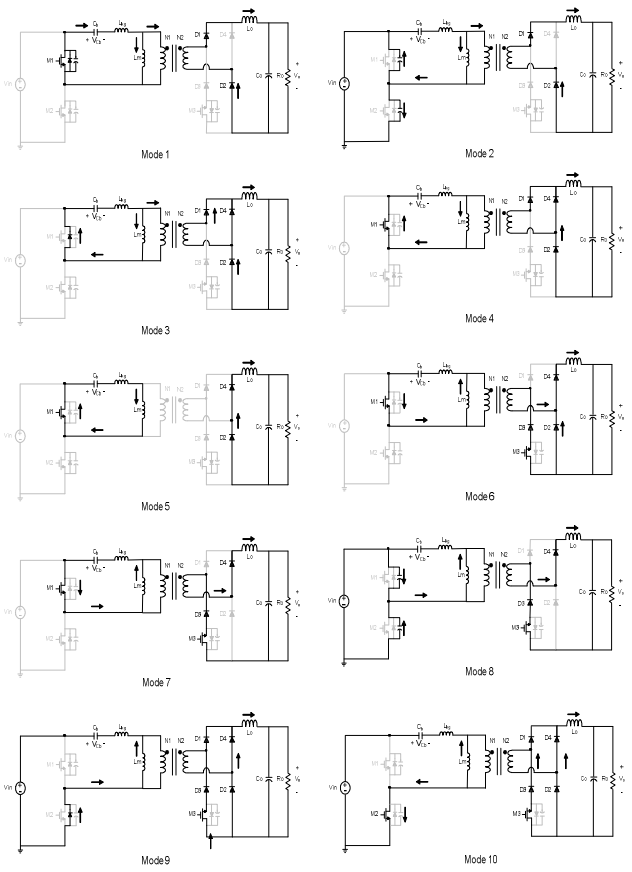

Fig. 3 Equivalent circuit of the proposed converter

$$i_{pri}(t) = nI_o + i_{Lm}(t) \tag{1}$$

$$i_{Lm}(t) = \frac{(1-D)V_{in}}{L_m}t + i_{Lm}(t_0) \tag{2}$$

where

$$i_{Lm}(t_0) = -\frac{(1-D)V_{in}}{2L_m}DT_s$$

During this mode, M3 is turned off with ZCS condition.

Mode 2(t_1~ t_2) : When M1 is turned off, this mode begins. Since $V_{ds2}(t)$ is higher than V_{Cb}, diode D3, D4 are still reverse biased. Therefore C_{oss1} and C_{oss2} are linearly charged and discharged, respectively. From the assumption (d), $i_{pri}(t)$ and $V_{ds1}(t)$ can be expressed as follows:

$$i_{pri}(t) = nI_o + i_{Lm}(t_1) \tag{3}$$

$$V_{ds1}(t) = \frac{i_{pri}(t_1)}{2C_{oss}}t \tag{4}$$

where

$$i_{Lm}(t_1) = \frac{(1-D)V_{in}}{2L_m}DT_s$$

Mode 2 ends at t_2 when $V_{ds1}(t)$ becomes equal to V_{Cb}

Mode 3(t_2 ~t_3) : After $V_{ds1}(t)$ increase to V_{Cb}, the output inductor current, $i_{Lo}(t)$ begins to freewheeling through D1,D2 and D4. Since the primary voltage across the transformer is 0V, $V_{ds1}(t)$ and $V_{ds2}(t)$ are charged and discharged, respectively, in matter of the resonance between L_{lkg} and C_{oss1}+C_{oss2}=2C_{oss} $i_{pri}(t)$ and $V_{ds1}(t)$ can be expressed as follows:

$$i_{pri}(t) = i_{pri}(t_2)\cos(\sqrt{\frac{1}{2L_{lkg}C_s}}t) \tag{5}$$

$$V_{ds1}(t) = i_{pri}(t_2)\sqrt{\frac{L_{lkg}}{2C_s}}\sin(\sqrt{\frac{1}{2L_{lkg}C_s}}t) + (1-D)V_{in} \tag{6}$$

After $V_{ds1}(t)$ and $V_{ds2}(t)$ reach V_{in} and 0V, respectively, i_{pri} (t) flows through the output diode of switch M2 and zero voltage across M2 is maintained. Therefore M2 can be turned on with ZVS condition at the next mode.

Mode 4(t_3~ t_4) : When M2 is turned on, this mode begins. Since commutation of secondary diodes does not complete, the voltage across the transformer is still 0V and V_{Cb} is all applied to the leakage inductor. Therefore, the leakage inductor current rapidly decreases as follows:

$$i_{pri}(t) = -\frac{DV_{in}}{L_{lkg}}t + i_{pri}(t_3) \tag{7}$$

where

$$i_{pri}(t_3) = \sqrt{i^2_{Lm}(t_2) - \frac{2C_s(DV_{in})^2}{L_{lkg}}}$$

Mode 5(t_4~ t_5) : When $i_{pri}(t)$ reaches $i_{Lm}(t)$, the output diode current completes its freewheeling. D1 is turned off and output current freewheels through D2,D4. Since V_{Cb} is applied to L_{lkg}+L_m , $i_{Lm}(t)$ can be expressed as follows:

$$i_{pri}(t) = -\frac{DV_{in}}{L_m}t + i_{pri}(t_4) \tag{8}$$

Mode 6(t_5~ t_6) : When M3 is turned on, this mode begins. Since secondary voltage of the transformer is zero, -V_{Cb} is applied to the leakage inductor. Therefore, $i_{pri}(t)$ rapidly decrease to reflected load current. $I_{pri}(t)$ can be expressed as follows:

$$i_{pri}(t) = -\frac{DV_{in}}{L_{lkg}}t + i_{pri}(t_5) \tag{9}$$

Mode 6 ends at t_6 when $I_{pri}(t)$-$I_{Lm}(t)$ becomes equal to I_O/n.

Mode 7(t_6~ t_7) : After -($I_{pri}(t)$-$I_{Lm}(t)$) becomes equal to I_O/n, D2 is turned off. The operation of this mode is similar to that of mode 1. $I_{pri}(t)$ can be expressed as follows:

$$i_{pri}(t) = -nI_o + i_{Lm}(t) \tag{10}$$

Mode 8(t_7~ t_8) : When M2 is turned off, this mode begins. The operation of this mode is similar to that of mode 2. Since $V_{ds2}(t)$ is smaller than V_{Cb}, diode D1, D2 are still reverse biased. Therefore C_{oss1} and C_{oss2} are linearly charged and discharged, respectively. From the assumption (d), $i_{pri}(t)$ and $V_{ds2}(t)$ can be expressed as follows:

$$i_{pri}(t) = -nI_o + i_{Lm}(t_7) \tag{12}$$

$$V_{ds2}(t) = \frac{i_{pri}(t_7)}{2C_s}t \tag{13}$$

where

$$i_{Lm}(t_7) = -\frac{(1-D)V_{in}}{2L_m}DT_s$$

Mode 8 ends at t_8 when $V_{ds2}(t)$ reaches to Vin - V_{Cb}.

Mode 9(t_8~ t_9) : The operation of this mode is similar to that of mode 3. After $V_{ds2}(t)$ increases over V_{Cb}, D1 and D2 are turned

on. Since the voltage across the transformer is 0V, $V_{ds1}(t)$ and $V_{ds2}(t)$ are discharged and charged respectively, in manner of the resonance between L_{lkg} and $C_{oss1}+C_{oss2}=2C_S$. Therefore $i_{pri}(t)$ and $V_{ds2}(t)$ can be expressed as follows:

$$i_{pri}(t) = i_{pri}(t_8)\cos(\sqrt{\frac{1}{2L_{lkg}C_S}}t) \tag{14}$$

$$V_{ds2}(t) = i_{pri}(t_8)\sqrt{\frac{L_{lkg}}{2C_S}}\sin(\sqrt{\frac{1}{2L_{lkg}C_S}}t) + (1-D)V_{in} \tag{15}$$

After Vds1(t) and Vds2(t) reach 0V and V_{in}, respectively, $i_{pri}(t)$ flows through the output diode of the switch M1 and zero voltage across M1 is maintained. Therefore M1 can be turned on with ZVS at the next mode.

Mode 10(t_9 ~t_{10}) : When M1 is turned on, this mode begins. The operation of this mode is similar to that of mode 4. Since commutation of secondary diodes does not complete, the voltage across the transformer is still 0V and V_{in} applied to the leakage inductor. Therefore, the leakage inductor current rapidly increases as follows

$$i_{pri}(t) = \frac{V_{in}}{L_{lkg}}t + i_{pri}(t_9) \tag{16}$$

where

$$i_{pri}(t_9) = \sqrt{i^2{}_{Lm}(t_8) - \frac{2C_s\{(1-D)V_{in}\}^2}{L_{lkg}}} \tag{17}$$

Mode 10 ends at t_{10} when $i_{pri}(t)$-i_{Lm} reaches I_O/n.

3. Analysis of the Proposed Converter

In this section, DC conversion ratio, offset of magnetizing current and ZVS conditions are presented.

A. DC conversion ratio

The DC conversion ratio of the proposed converter can be expressed as follows:

$$V_O = D\times\frac{N_2}{N_1}(1-D)V_{in} + D\times\frac{N_2}{N_1}DV_{in} = \frac{DV_{in}}{n} \tag{18}$$

B. DC offset of magnetizing current

The DC offset of magnetizing current can be calculated by applying current-second law to C_b. It can be expressed as follows:

$$D(I_{Lm}+\frac{I_o}{n}) = D(-I_{Lm}+\frac{I_o}{n})$$
$$\therefore I_{Lm,DC\ offset} = 0 \tag{19}$$

C. ZVS conditions

ZVS Condition of M1can be expressed as follows:

$$\frac{1}{2}L_{lkg}I_{pri}(t_3)^2 > 2C_s\{(1-D)V_{in}\}^2$$
$$\frac{1}{2}L_{lkg}\{\frac{D(1-D)V_{in}}{2L_m}+\frac{I_o}{n}\}^2 > 2C_s\{(1-D)V_{in}\}^2 \tag{20}$$

ZVS Condition of M2 can be expressed as follows:

$$\frac{1}{2}L_{lkg}I_{pri}(t_9)^2 > 2C_s(DV_{in})^2$$
$$\frac{1}{2}L_{lkg}\{\frac{D(1-D)V_{in}}{2L_m}+\frac{I_o}{n}\}^2 > 2C_s(DV_{in})^2 \tag{21}$$

4. Experimental Results

To verify operation of the proposed converter, a prototype circuit has been designed for the specification as follows:

- rms ac input voltage $V_{in,rms}$: 110~220V_{rms}
- output voltage : 48V
- maximum output power $P_{o,max}$: 200W
- switching frequency : 100kHz

Fig. 5 shows the experimental waveforms at V_{in}=110V_{rms}. ZVS operations of primary main switches are easily achieved by reflected load current. Switch (M3) is turned on and off with ZCS. Fig. 6 shows the experimental waveforms at V_{in}=220V_{rms}. There are no dc offset of magnetizing current although duty is very small. Therefore, ZVS operations of primary main switches are easily achieved by load current without interference of magnetizing current.

The measured efficiency of the proposed converter are from 84%(V_{in}=110V_{rms}) to 88%(V_{in}=220V_{rms}) at full load

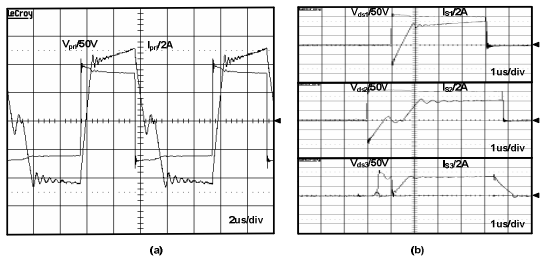

Fig. 4 Experimental Waveforms at V_{in}=155V
(a) V_{pri}, I_{pri} (b)V_{ds1}, I_{M1}, V_{ds2}, I_{M2}, V_{ds3}, I_{M3},

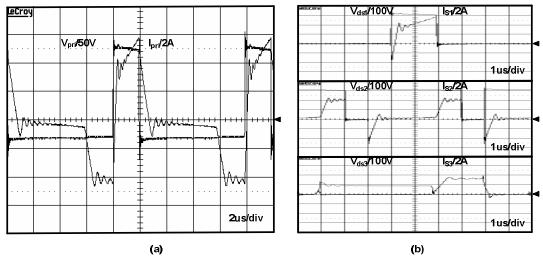

Fig. 5 Experimental Waveforms at V_{in}=310V
(a) V_{pri}, I_{pri} (b)V_{ds1}, I_{M1}, V_{ds2}, I_{M2}, V_{ds3}, I_{M3},

4. Conclusion

This paper has presented the analysis and experimental results of the proposed half bridge converter without DC offset of magnetizing current. It has no DC offset of magnetizing current according to duty ratio. Therefore, it has low conduction loss and guarantees the ZVS operations of primary main switches in wide input range. The experimental results of a 200W prototype converter has proved the key characteristics of the proposed converter in wide input range.

Reference

[1] Hong Mao, " A new duty-cycle-shifted PW< control scheme for half-bridge DC-DC converters to achieve zero-voltage-switching", Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2003, Vol. 2, pp. 629-634.

[2] Hong Mao, "Zero-voltage-switching half-bridge DC-DC converter with modified PWM control method", IEEE Transactions on Power Electronics, Vol. Issue 4, July 2004, pp.947 - 958

[3] Jiangtao Feng, "ZVS analysis of asymmetric half-bridge converter", PESC, 2001, pp.243-247.

[4] Sebastian, J. "An overall study of the half bridge complementary control DC to DC converter", PESC, 1995, pp.1229-1235.