전류 Stress 최소화 제어설계를 응용한 PFC Boost Pre-regulator

이희철, 김정은, 박홍선, 박기범, 문건우

Current Stress Minimizing Control Scheme for Power Factor Correction (PFC) Boost Pre-regulator

Hee-Chul Lee, Chong-Eun Kim, Hong-Sun Park, Ki-Bum Park, Gun-Woo Moon

ABSTRACT

A simple technique for PFC circuit is presented using UC3854. This technique is about current peak controlling by a reference current generator. Decreased peak currents of the boost pre-regulator reduce circuit current stress and so rated currents of circuit elements are minimized. Simulation and experimental results will verify the viability of the new scheme.

Key Words : PFC, UC3854, CCM, boost converter, harmonics

1. Introduction

Power factor correction (PFC) circuits have been developed to use electric devices during past few years. A conventional capacitive bridge rectifier induces much harmonic currents, therefore it needs to rule world-wide current harmonic limits. The IEC Std. 61000-3-2 is representative regulation agreement for PFC [1].

There are several types of PFC circuits and here we refer two-stage active PFC which composed of both boost pre-regulator circuit and DC-DC converter. Generally the boost circuits are controlled with current mode control. And these are classified with CCM, BCM and DCM. PFC boost pre-regulator in CCM shows low peak current characteristic and so conduction loss and conduction noise decrease more than BCM, DCM [2]. However, PFC circuit controlled by CCM has still high peak current therefore effects harms for current stress in overall circuit which is composed of inductor, switch, and diode [3].

To suppress the current stress more, the novel peak reducing technique for PFC is proposed and it can be achieved by only inserting a zener diode. Therefore, the current rating of semiconductor and magnetic devices can be reduced. Moreover, the output capacitor voltage ripple can be also reduced. For validity of proposed scheme, simulation and experimental results are presented.

2. Operation principle

Theoretically reference current follows line voltage waveform in conventional PFC circuit with UC3854 controller. Proposed control technique is to make a reference current I_{REF} which clamped and decreased peak $m\times I_{REF,\ PEAK}$ by using a zener diode. We define m as scaling factor of peak value of I_{REF} and also define t as scaling factor of I_{IN} in Fig. 1. Of course, I_{IN} may follow I_{REF} waveforms very well by UC3854.

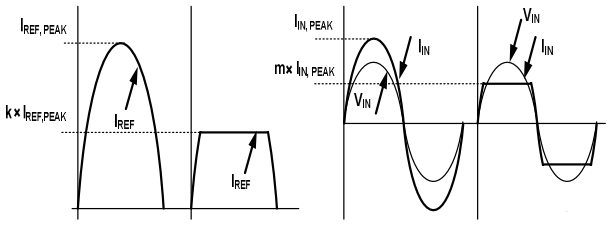


Fig. 1 Proposed peak current waveforms,
(a)Reference current waveforms,
(b) Line voltage and current waveforms

Generally boost PFC circuit has multiplier, voltage compensator, current compensator and reference current generator. This multiplier creates the current programming signal I_{AC} by multiplying the rectified line voltage V_{REC} with the output of the voltage error amplifier so that the current programming signal I_{AC} has the shape of the input voltage V_{IN} and average amplitude which controls the output voltage V_{OUT} in Fig. 2.

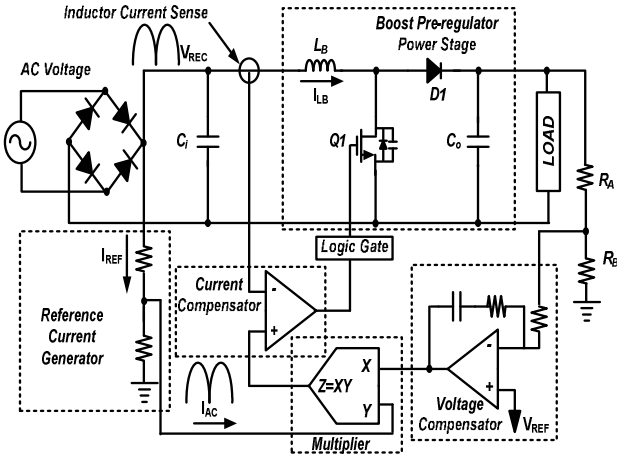
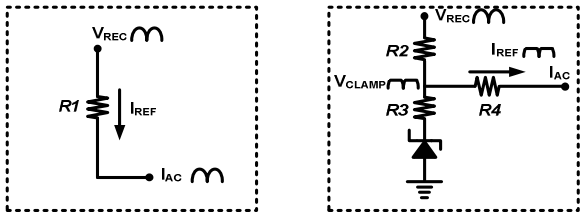


Fig. 2 Active Boost Power Factor Correction Circuit

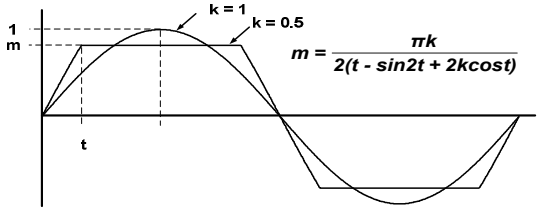
We especially replace the reference current generator to get decreased current peak in Fig. 3. It shows reference current I_{REF} is induced from V_{REC} and then it flows to I_{AC} of UC3854. A zener diode clamps V_{REC} and this clamped current flows to I_{AC} in proposed circuit.



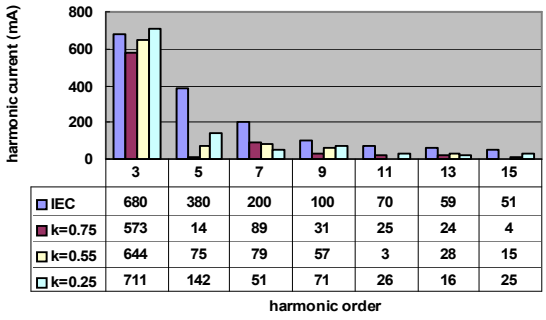
(a) (b)

Fig. 3 Refenence current generator circuit,
(a) Conventional circuit,
(b) Proposed circuit

These clamped sine current waveforms are different from pure sine waveforms. Theoretically when value k is smaller, the harmonic currents become larger. Fig. 4 shows correlation of both k and m according to duration time and simulation values are compared with the IEC limiting values. Simulation proves that proposed controller is acceptable for harmonic current limits at k=0.55 and has reduced peak current in case of 200 W, 90 V_{AC} ~ 270V_{AC} universal line input in Fig. 4.



(a)



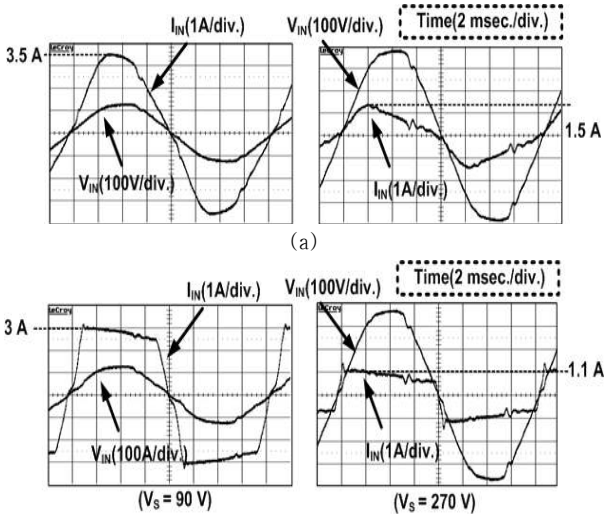
	3	5	7	9	11	13	15
IEC	680	380	200	100	70	59	51
k=0.75	573	14	89	31	25	24	4
k=0.55	644	75	79	57	3	28	15
k=0.25	711	142	51	71	26	16	25

(b)

Fig. 4 Harmonic currents comparison,
(a) Current waveforms according to k ,
(b)Harmonic currents according to k

3. Experimental results

Experiment of 200 W, 90 V_{AC} ~ 270 V_{AC} PFC circuit is implemented. Fig. 5 shows conventional and proposed waveforms, and it shows line current I_{IN} peak value is improved by proposed controller. Data of Both 90 V_{AC} and 270 V_{AC} have same experimental results concerning as peak decreasing. Line input current I_{IN} decrease 14% from 3.5 A to 3 A at 90 V_{AC}.



(a)

(b)

Fig. 5 Input voltage and current waveforms,
(a) Conventional circuit,
(b) Proposed circuit

The boost inductor current I_{LB} decreases 20% from 4 A to 3.2 A at 90 V_{AC} in Fig. 6 like the line current I_{IN} does.

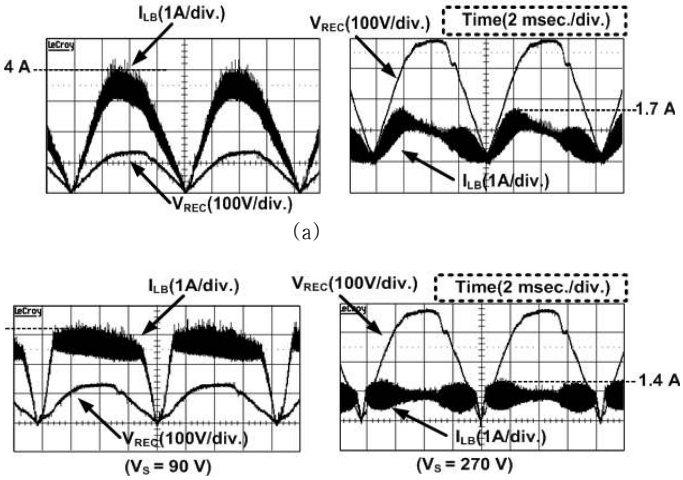


Fig. 6 Rectified voltage and current waveforms,
(a) Conventional circuit,
(b) Proposed circuit

Moreover, output capacitor can be minimized due to voltage ripple decrease 20% from 8 V to 6.4 V at 270 V_{AC}. We can tell controller is superior to conventional controller in case of current peak reducing and output voltage ripple.

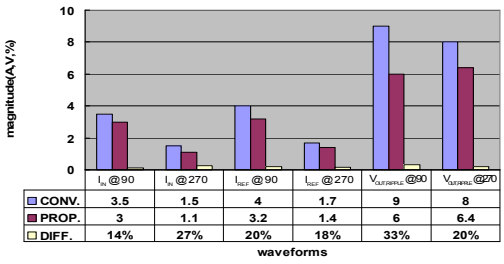
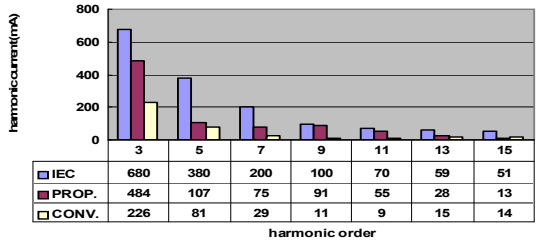
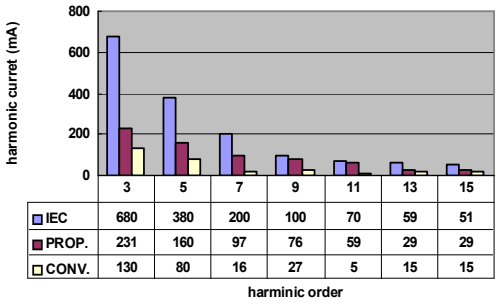


Fig. 7 Peak and ripple values comparison

Next in Fig. 8, harmonic currents are compared both of controllers with the IEC regulation values. Even though the proposed controller increases harmonics more or less, it satisfies the IEC Std. well.



(a) Vs = 270 V



(b) Vs = 90 V

Fig. 8 Harmonic current comparison

5. Conclusions

For better PFC boost converter, this digest shows the new technique to decrease the current peak and voltage ripple. Decreasing peak currents of the boost pre-regulator influences on reducing circuit current stress and then rated current of circuit elements can be minimized. The practical guideline is suggested for application for 1 kW 63inch PDP TV as following experiment.

References

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