Rigid and flexible displays with solution processed dielectric passivation layer integrated with E-Ink imaging films

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Abstract

Organosiloxane based spin on planarizing dielectrics (PTS-E and PTS-R) were developed for application in flat panel displays as a replacement to conformal chemical vapor deposited SiNx. Here we demonstrate the successful use of siloxane-based material as a passivation layer for active matrix α-Si thin film transistors (TFT) on both rigid and flexible substrates.

1. Introduction

Traditionally SiO_2-based hybrid dielectrics with dielectric constant of <3.9 is used in microelectronic circuits to reduce capacitive coupling and increase the speed of operating devices. These materials contain organic groups attached to Si in SiO2 framework and these are usually deposited by chemical vapor deposition. The dielectric is used to insulate adjacent metal lines and vias on the same layer (intra-layer dielectric) or on two different layers (inter-layer dielectric). Flat panel display industry has adopted most of the materials and technology from microelectronic industries to build flat panel display screens. Traditionally the dielectric in flat panel displays is SiN_x or SiO_2 and is deposited by plasma enhanced chemical vapor deposition (PECVD). This method of deposition gives rise to conformal coating (uniform thickness over the topology of the underlying layer). These materials were traditionally chosen due to their good electrical performance, for example, SiN_x is the most commonly used film for gate dielectric and interlayer dielectric in the thin film transistor (TFT) that functions as the on/off switch in flat panel screens [1]. However, when the topology of the surface and the substrate size (with generations) are large, chemical vapor deposition cannot meet the requirements of cost and planarization of surface [2].

Solution-based coating of dielectric materials are able to planarize surfaces with topographies (be it a TFT array glass or color filter panel) and provide a flat surface on which LCD, OLED or electrophoretic layers can be easily and more efficiently integrated. Patterning precision is also improved by using solution-based coating methods. Flat panel display industry is open to solution based coatings unlike microelectronic industries because of the sheer size of the panels, high cost associated with CVD and larger device dimensions (>5µm size) with the associated less stringent electrical requirements. Solution processed materials are also attractive for flexible displays due to compatibility with roll to roll processing and the ability to allow the substrate to bend without the film cracking, which would happen with a PECVD inorganic film.

There are well-documented reports on the performance and reliability of microelectronic devices formed of interconnects (metal and dielectric layers) with hybrid SiO_2–organic (commonly known as CDO – carbon doped oxides of silicon) dielectrics. The major issue is caused by the dielectric damage upon exposure to wet etching, plasma treatments, resist strip, wet cleans and so on. The display panels are not far off from these requirements. Dielectric materials with organics built in Si-O framework deposited from solutions are expected to exhibit resistance to wet chemical and plasma etch processes, and photoresist (PR) strip and wet clean processes. Table 1 lists the main properties required for ILD applications in LCD, OLED and electrophoretic flat panel displays.

Table 1: Property sets required from a TFT passivation or ILD material

Properties	TFT passivation / ILD
Thermal Budget / process or cure temperature	~ 400°C (LTPS) ~ 350°C (a-Si) < 200°C (organic semiconductor and flexible substrates)
Film Thickness	From 1.5µm to 3.5µm
Transmittance	> 95%
Planarization	> 95%
Resistance to plasma induced damage	Fluorine-based plasma (SF_6, CF_4, CHF_3), O_2 plasma used for PR ash
Wet chemical resistance	ST106, PRS2000, N300, TMAH, KOH and so on
Adhesion	Al, Cr, ITO, SiN, organic layers
Outgassing	Low (less than typical CVD chamber pressure)
H_2O / O_2 diffusion	Low
Dispense tool	Spin or slot die coaters, screen printers, spray coating

2. Experimental

Material Characterization

Dielectric formulations (Planarizing and Thermally Stable-PTS) comprising organic siloxanes were prepared in organic solvents and spin-coated on to silicon or glass wafers. In this paper, results from two different products PTS-E and PTS-R are discussed. Both materials were hot-plate baked at 160°C/200°C for 1 min each and cured at 200°C for 1 hr in a furnace in a N_2 environment. However, various combinations of bake/cure conditions are possible to form dielectric films for different applications.

The dielectric properties were measured using a mercury probe at 100 kHz frequency. Film thickness was measured after bake and after cure using Thermawave® to calculate the film shrinkage due to curing. Refractive index (RI) of the film was also measured after bake and cure. Thermal stability was measured using a Thermal Desorption Mass Spectroscopy (TDMS) with the wafer maintained at cure temperature. Wafers were sliced into small pieces and immersed in wet chemistries for a fixed period of time to characterize wet etch resistance. Dry etch methods were developed to pattern the dielectric film. Adhesion to different layers (metals, other dielectric films, organic films) was measured using a standard tape test.

PTS-E and R were coated on Gen 2 size glass panels using a Tazmo slot die coater. Properties tested were film thickness, % uniformity and presence of mura.

TFT Fabrication

Full devices were prepared by the Flexible Display Center at Arizona State University (FDC). The FDC employs an inverted staggered trilayer, channel passivated thin-film transistor structure. Arrays were fabricated on silicon and planarized SS430 stainless steel. PTS-E or R was deposited as a 2 µm thick layer on top of the TFT structure and cured at 180°C to form the dielectric film. Mo and ITO were used to form the pixel electrodes.

3. Results

Material Properties

PTS-E and PTS-R were found to have film characteristics that are well suited for TFT passivation layers for glass, silicon, plastic and stainless steel substrates. Film shrinkage from bake to cure is low (< 3%) for these materials indicating that the films have low stress. Refractive index was 1.49 for PTS-R and 1.55 for PTS-E, both well matched to glass which reduces light loss due to internal reflection at the interfaces. PTS-E and PTS-R films were found to have high optical transparency, greater than 95% over a broad range (400 to 1000nm) of wavelengths.

Both film types were hydrophobic, with contact angles of ~90°. Adhesion of both films PTS-E and PTS-R is good with other films (metal, other dielectric layers and organic layer) commonly used in a standard display panel.

As listed in Table 2 the dielectric materials have a k value of ~ 3 to 3.3. Breakdown strength of the dielectrics (measured at 1µA current) is high in the range of 4.4 to 5.0 MV/cm. Leakage current density measured at 2MV/cm is 25 to 90nA/cm^2. Low dielectric constant and high thickness (up to 3.5µm) of these films lead to superior performance over the traditional PECVD ILD films.

Table 2: Dielectric properties of PTS-E and PTS-R

Material	Dielectric constant, k	Field at 1µA (FBD), MV/cm	Current density at 2MV/cm (A/cm^2)
PTS-E	3.09	4.5	8.90E-08
	3.08	4.39	7.06E-08
PTS-R	3.3	4.79	2.49E-08
	3.31	4.7	2.37E-08

Films were coated with high degrees of uniformity for both spin coat and slot die coat deposition methods. Film showed no striations or interference mura.

One of the main requirements of a display dielectric is low out-gassing and resistance to moisture absorption and diffusion. Figure 1 shows the outgassing profile of 200°C-cured PTS-R film. Cured films were loaded in a thermal desorption mass spectrometer and the temperature was ramped to 180°C or at 10°C/min and held there for an hour. The Figure shows the outgassed components and their intensity in terms of pressure. The main outgassed component is water. Total out-gassing is very low of the order of 5x10^{-8} Torr.

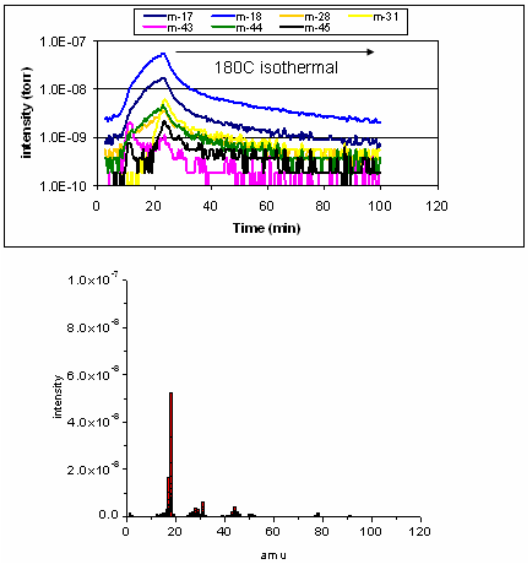

Figure 1. Outgassing profile for 200°C cured PTS-R film

Device Performance

There was very little difference in the transfer and output characteristics for fabricated transistors on either silicon or stainless steel substrates. Saturation mobilities and on/off ratios rivals that of previously reported high temperature processes [3]. Electrical characteristics are summarized in Table 3.

Table 3. Characteristic TFT Properties on SS430

Saturation Mobility	0.70 cm^2/V-sec
Threshold Voltage	1.6 V
Sub-Threshold Slope	0.49 V/decade
On/Off Ratio (20Vds, 0Vgs)	$1.28x10^6$
On/Off Ratio (20 Vds, -15Vgs)	$8.08x10^8$
Hysteresis	0.31 V

Displays were created by attaching E Ink® Vizplex 100 imaging film as well as gate and source drivers to either debonded, singulated stainless steel or silicon substrates. In both cases, PTS-E and PTS-R films were found to give superior performance over SiN as the passivation layer, as demonstrated in figure 2. The PTS-E and PTS-R Full Flow display had clearer images with crisper edges as well as a better range of grey scale. The SiN ILD Full Flow displays did not function as well as the PTS-E/PTS-R ILD Full Flow displays. Images that were driven with black or dark grey would fade out to light grey/white. Consecutive runs improved functionality of this display. Also, no cross talk is visible. Cross talk used to be an issue for black images driven on the same column line with a white background, especially when integration is stopped at the S – D level.

4. Conclusion

The dielectric material family developed at Honeywell Electronic Materials meets all the property requirements of display dielectric films for rigid and flexible displays such as hydrophobic surface, low cure temperature, high thermal stability with associated low outgassing, moisture absorption, and penetration resistance, very high planarization, optical transmittance, low dielectric constant (κ=3.1 to 3.3), good electrical properties, high crack threshold (as high as 3.5 μm), high planarizing ability, resistance to photoresist strip and ash chemistries and a very smooth surface.

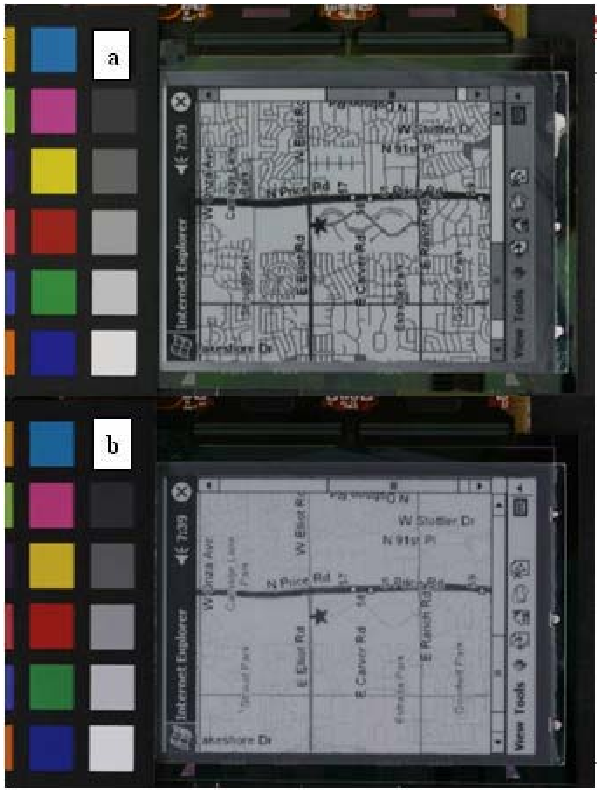

Figure 2. 3.8-inch QVGA active matrix electrophoretic display on silicon substrate using (a) PTS-E or (b) SiN as passivation layer

5. References

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