Cost Effective 60Hz FHD LCD with 800Mbps AiPi Technology

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Abstract

AiPi technology incorporates an embedded clock and control scheme with a point-to-point bus topology, achieving the smallest possible number of interface lines between a timing controller and source drivers. A 46" AiPi-based 10-bit FHD prototype requires only 20 interface lines, compared to 38 lines for mini-LVDS. The measured maximum data rate per one data pair is more than 800Mbps.

1. Introduction

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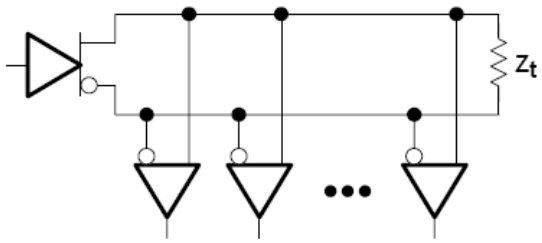
LCD displays have provided end-users with outstanding performance including high brightness, high contrast, wide color gamut, slim and light design, and other benefits. Still, display markets continue to demand more advanced technologies such as higher resolution, higher driving frequency, and higher color bit depth.

For TV applications, some panel makers have exhibited large size LCDs in 2007 with resolution of 3840x2160 (QFHD, or UD). For monitor applications, 3200x2400 (WQUXGA) displays will be released this year. To achieve higher motion picture quality, 120Hz driving technologies have been applied to LCD TVs with motion estimation and motion compensation (MEMC) algorithms [1]. Those schemes have improved the motion blur characteristics and most panel or TV makers are following this move. Furthermore, because the display quality has been more important as the display size and resolutions have increased, higher bit depth displays have been studied [2]. Also, in order to adjust the gammas of red, green, and blue pixels separately, higher bit depths have been proposed with linear digital to analog converter (DAC) source drivers [3].

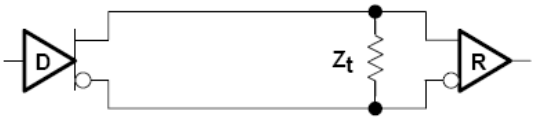
These demands increase the number of interface lines in display systems due to higher data rates, resulting in negative impacts to cost, power consumption, and EMI.

In the area of system interfaces, low voltage differential signaling (LVDS) has been used and recently, new high speed serial interfaces like DisplayPort (DP) and V-by-One have been developed to reduce the number of interface lines [4][5][6].

In the area of intra-panel interfaces, reduced swing differential signaling (RSDS) and mini low voltage differential signaling (mini-LVDS) have been the main interfaces in use until now.



(a) Multi-drop connection



(b) Point-to-point connection

Figure 1. Bus topologies of intra panel interfaces

As shown in Figure 1(a), existing RSDS and mini-LVDS interfaces have adopted a multi-drop bus topology with several stubs, causing impedance mismatching. Because this mismatching reduces the timing margin of transmitted and received data due to

signal reflection, high data rates can not be supported. Recently, to cope with this limitation, point-to-point interfaces have been proposed and developed for use as the intra-panel interface [3][7].

In general, a point-to-point interface comprised of one TX and one RX, as shown in Figure 1(b), can obtain good impedance matching as well as faster data rate because there are no stubs on the interface bus lines. However, existing point-to-point interfaces forward the clock separately, which can result in skew problems between clock and data signals. At higher data rates the sampling window is narrower, therefore skew becomes more critical. Therefore, current point-to-point solutions require additional complex circuitry to adjust the phase of the sampling clock, which increases the size and cost of the system, or alternatively they use multiple data pairs for the point-to-point link. An advanced intra panel interface (AiPi), which is a clock embedded point-to-point interface, was first introduced at SID2006 for use in an HD application as a solution to the skew problem between clock and data signals [8]. This paper describes enhanced AiPi technology for use in FHD applications.

2. Advanced Intra Panel Interface

2.1 Clock Embedded Data

AiPi establishes a cost effective solution by means of a point-to-point bus topology and an embedded clock and control scheme. The skew issue between data and clock signals is eliminated by means of the embedded clock scheme, in which the clock signal is sent via the data line. Because clock and data signals have the same path, there is no skew therefore additional de-skewing circuitry is not necessary. AiPi makes use of multi-level signaling as shown in Figure 2.

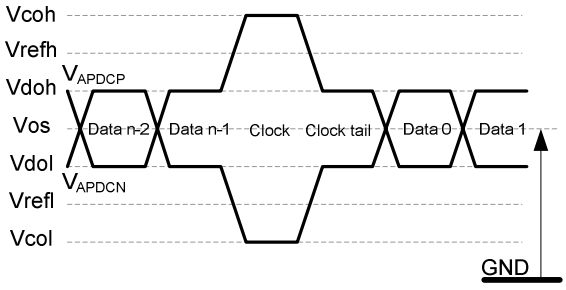


Figure 2. Multi-level signaling for an embedded clock scheme

This method can be implemented by a simple clock data recovery (CDR) circuit. CDR detects the signal as the clock when the input level is higher than Vrefh or lower than Vrefl. The signal within the range from Vrefl to Vrefh is treated as data.

The clock tail bit is inserted just after the clock pulse to reduce the effect of inter-symbol interference (ISI). The polarity can be changed by setting the internal register of the AiPi transmitter. Because the clock information is extracted at the rising edge crossing over Vrefh and the falling edge crossing over Vrefl, CDR performance is not impacted by jitter caused by the polarity of the clock tail bit. At low data rates, the clock tail has the same polarity as the clock to reduce the transition voltage, and at the high data rates, the clock tail has a polarity opposite that of the clock to reduce ISI.

Clock pulses of high amplitude are added twice per one serialized pixel data as described in Figure 3 to reduce the number of delay stages in the delay locked loop (DLL). 10-bits of red data and the 4 MSBs of green data are transmitted first and then the remaining data are sent between clock pulses. This embedded clock scheme also helps reduce the number of lines between the TCON and source drivers as there is no need for dedicated clock lines.

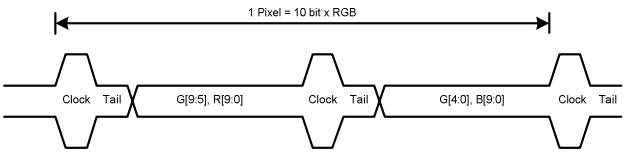


Figure 3. One pixel data transmission on AiPi

2.2 Control Embedded Data

In general, because source drivers need timing information about the beginning of each horizontal line, panel driving, and the pixel polarity, the TCON to source driver interface requires some additional lines. RSDS provides three control signals, STH, TP, and POL, while mini-LVDS has two control signals, TP and POL. However, AiPi technology can generate the data stream including the control signals without requiring additional lines. A data enable (DE) signal, following the clock tail bit, indicates whether the serialized data are image data or not. If the DE bit is high, the stream that follows is pixel data, and if DE is low, blanking or control data is transferred as shown in Figure 4. The information about beginning of horizontal line is extracted from the DE transition and

the rising edge timing and pulse width of TP and the level of POL are assigned to the first data of a low DE period. Also, source driver control signals can be programmed separately due to the point-to-point bus topology.

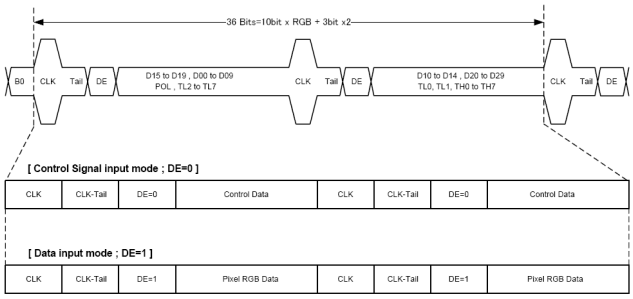


Figure 4. AiPi data mapping protocol

3. Implementation and Measurement

The AiPi proto-type was built on a 10-bit 60Hz 46" FHD LCD. The AiPi source driver was fabricated in NECEL's 0.35-um process by replacing the mini-LVDS RX with the AiPi RX in an existing 10-bit 576-ch mini-LVDS source driver. Only one AiPi data pair was implemented in the source driver. The AiPi timing controller board is shown in Figure 5. The total number of interface lines between the TCON and the 10 source drivers is 20, compared to 38 intra-panel interface lines for mini-LVDS, as shown in Table 1.

Figure 5. Photographs of TCON board

Table 1. Comparison of mini-LVDS and AiPi in 60Hz FHD

	Mini-LVDS	AiPi
Data	32 lines	20 lines
Clock	4 lines	0 lines
Control	2 lines	0 lines
Total	38 lines	20 lines

Because the multi-level signaling of AiPi is more sensitive to the fluctuation of the common mode voltage, a termination with two 50 ohm resistors and one capacitor was adopted as shown in Figure 6.

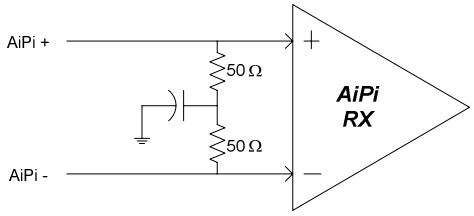
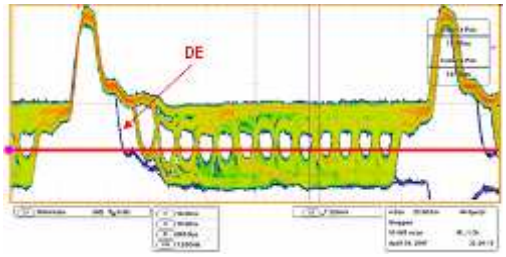
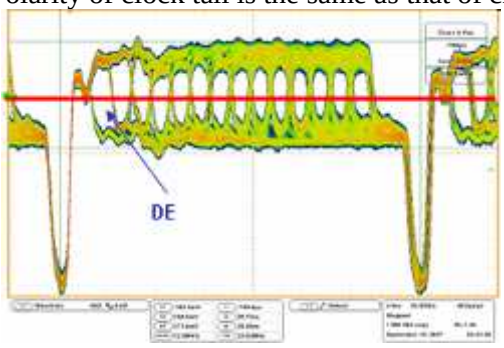


Figure 6. Termination of AiPi signal pair

Figure 7 shows the measured eye diagrams when the polarity of clock tail has same and opposite polarities of the clock pulse. As explained above, in the case of the same polarity, the ISI component of the clock deteriorates the DE bit, resulting in error. However, the opposite polarity reduces the effect of clock's ISI and helps the AiPi RX extract the correct value of the DE bit.



(a) Polarity of clock tail is the same as that of clock



(b) Polarity of clock tail is opposite to that of clock

Figure 7. Eye diagrams at the input of source drivers

Maximum pixel frequencies were measured over 30 source drivers as shown in Figure 8 and the data rate can be obtained by Eq. 1, showing that most of the source drivers can support a pixel frequency higher than 220MHz, which is equivalent to a data rate of higher than 800Mbps for one AiPi data pair. Figure 9 shows the proto-type 10-bit 46" FHD display.

$$DataRate_{AiPi} = \frac{Freq_{PixelClock} \cdot (BitDepth \cdot 3 + 6)}{\#\ of\ \ Source\ \ Drivers} \quad \text{(Eq. 1)}$$

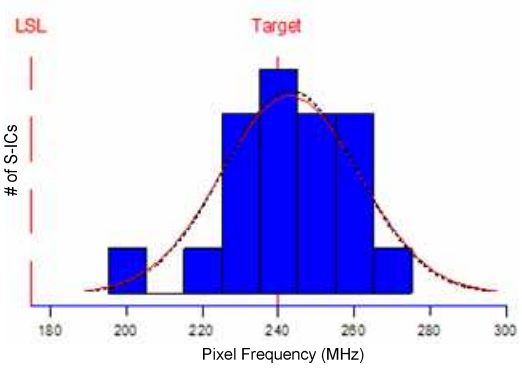
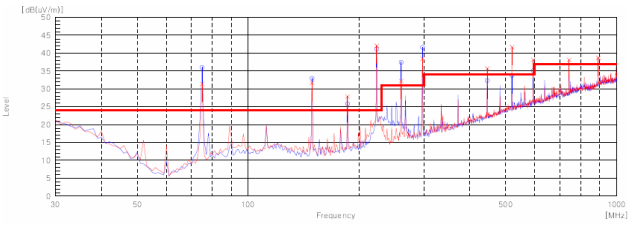
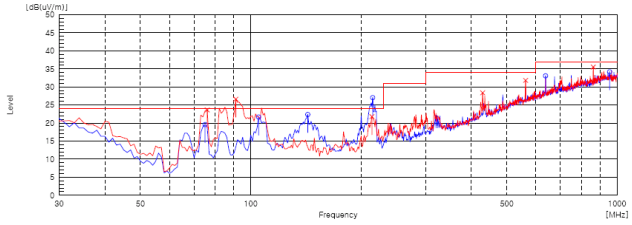


Figure 8. Histogram of measured maximum pixel frequency

Figure 9. Proto-type 10-bit 46” FHD display



(a) mini-LVDS



(b) AiPi

Figure 10. EMI comparison between mini-LVDS and AiPi

Figure 10 shows the EMI comparison between mini-LVDS and AiPi with 2-layer PCBs at 60Hz FHD. As expected, an AiPi technology with its slim interface can dramatically improve EMI performance.

4. Summary

AiPi technology reduces the number of intra-panel interface lines by using a point-to-point bus topology and by elimination of the clock and control signal lines. The proto-type 10-bit 46” FHD LCD reduces the interface lines between TCON and source drivers to 20 lines, compared to 38 lines for mini-LVDS. The maximum data rate was measured as higher than 800Mbps, which means a pixel clock frequency of up to 220MHz can be supported. This feature reduces the TCON and PCB costs, and improves EMI performance.

5. References

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