Oxide Semiconductor TFTs for the Next Generation LCD-TV Applications

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Abstract

For a large sized , ultra definition (UD) and high refresh rate for motion blur free AMLCD TVs, amorphous IGZO thin film transistor (TFT) are applied and investigated in terms of threshold voltage (V_{th}) shift influenced by active layer thickness uniformity, source drain etching technology, heat treatment and passivation condition. Optimizing above parameters, we fabricated the world's largest 15 inch XGA AMLCD successfully.

1. Introduction

As the application of LCD requires high quality performances, such as high resolution, fast response, and embedded integrated driving circuit, high mobility TFTs have attracted considerable attention to chargeability. In case of ultra definition (UD) AMLCD-TV, conventional a-Si TFT limits the operation of the 82-inch at 60Hz [1]. However, in order to drive the LCD at higher frequencies such as 120, 240Hz etc., field effective mobility at least $3cm^2$/V-s is required because shorter pulse time is needed to charge the pixel.

Oxide semiconductor thin film transistors are one of the most promising candidates for this in the research and development stage. Recently, an IGZO oxide thin film transistor (TFT) has been introduced as one of the most promising candidates for flexible displays and active-matrix organic light emitting diode (AMOLED) TV because it has high mobility of $10{\sim}40cm^2/(V{\cdot}sec)$, an amorphous structure and low thermal budget process[2-3]. However, in terms of mass production for large size, high performance TFT -LCD displays on the large glass substrates (>Gen 8), threshold voltage (V_{th}) uniformity control become of most important subject. This paper describes the effect of IGZO thickness, source/drain (S/D) etching process and passivation process on V_{th} variation of TFTs. We have demonstrated a 15-inch XGA AMLCD panel using the IGZO TFT array.

2. Experimental

Bottom gate back channel etched TFTs were fabricated using $300x400mm^2$ glass substrates. To measure the uniformity of TFT transfer characteristics, 7x5 test element groups (TEGs) which have various kinds of TFTs were designed within $260x360mm^2$ size on a glass substrate. Molybdenum (Mo) was deposited by sputtering as both gate and source and drain (S/D) electrodes. IGZO (In:Ga:Zn = 2:2:1) layer with an average thickness of 700Å was deposited by sputtering equipment. SiNx (4500Å) film was deposited by plasma enhanced chemical vapor deposition (PECVD) as a gate insulator. Both wet and dry etching techniques were applied for S/D patterning. SiOx (2000Å) film was deposited as a passivation layer by PECVD.

3. Results and Discussion

Two kinds of devices were employed as shown in

Figure 1(a) and (b) in order to separate passivation effect on I_d-V_g characteristics of IGZO. Furnace annealed was followed after TFT fabrication in air at 250℃. A dual annealing process was applied in the structure of Fig 1(b) to minimize the influence of previous process conditions. This procedure involves annealing of the TFTs after S/D etching and additional annealing after TFT fabrication. Compared to etch stopper structure, no additional mask process is needed. Hence IGZO TFT array can be realized without increasing process complexity (5-mask normal) or cost for TFT-LCD display.

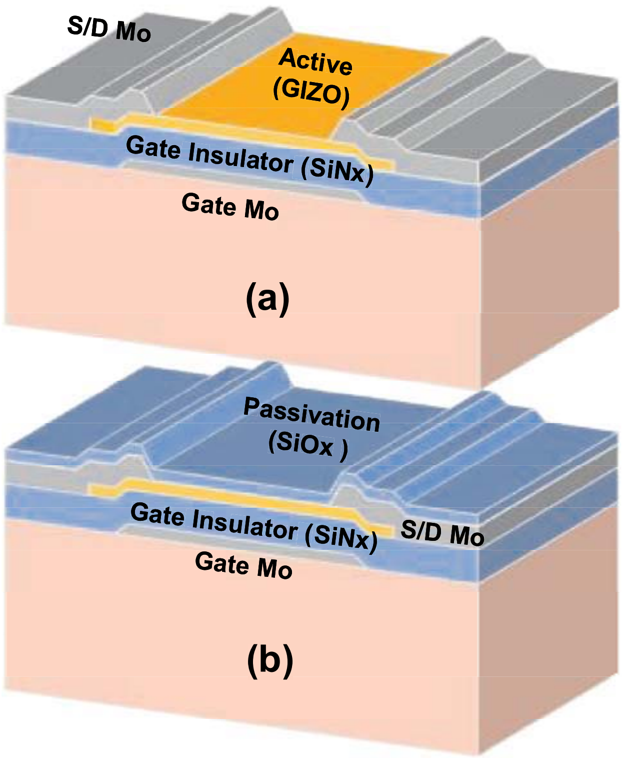


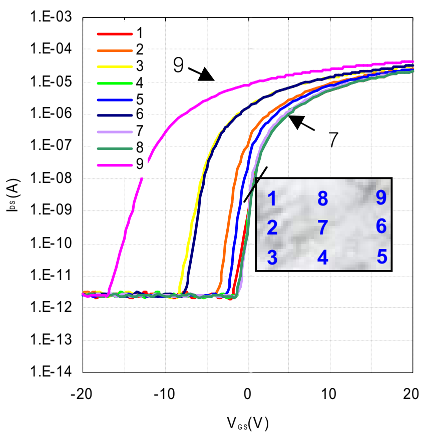
Fig 1. Schematic diagram of inverted bottom gate structure IGZO TFTs, (a) without and (b) with a passivation layer, respectively

Table 1 shows the etching rates of S/D Mo and IGZO layer and etching selectivity between them for wet and dry etching process respectively. During the wet etching of S/D, IGZO under layer was also etched so the IGZO channel thickness was carefully controlled to have around 550Å thickness, which is less than initial thickness of 700Å. However, for dry etching process of S/D, initial thickness of IGZO was almost the same as that of the channel region due to

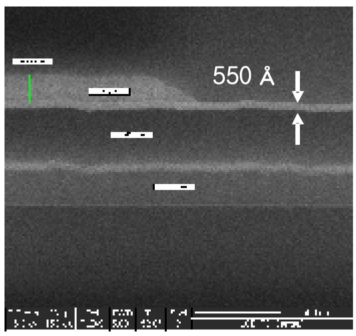
Table 1. Etching characteristics of Mo and IGZO with respect to S/D etching mode.

	Wet etching	Dry etching
Etching rate of Mo (Å/sec)	100~150	30~40
Etching rate of IGZO (Å/sec)	10~30	2~3
Etching selectivity of Mo with respect to IGZO	5:1~10:1	10:1~20:1

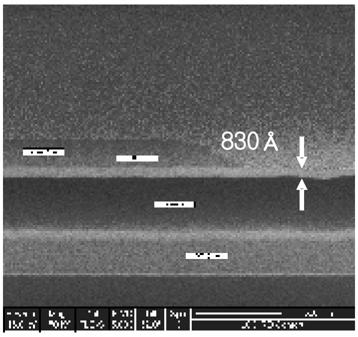
the slow etching rate and high etching selectivity. Dry etching selectivity was mainly dependent on gas chemical composition and plasma power when the plasma mode was fixed. Fig. 2 (a) shows TFT transfer curves at 9 points over a glass after S/D dry etching and post annealing processes without passivation. The



(a)

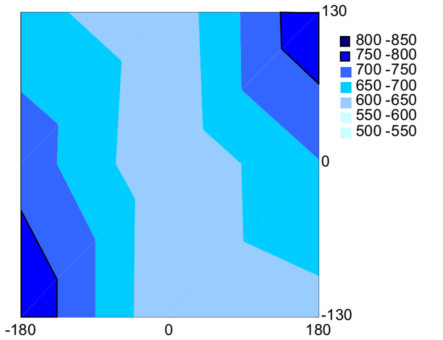


(b)

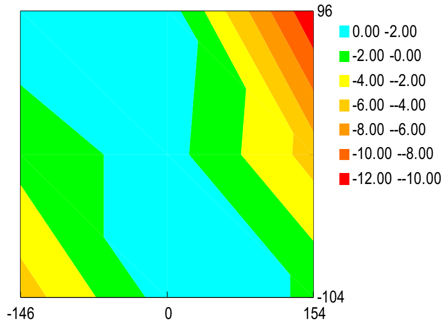


(c)

Figure 2 (a) Transfer curves of TFTs of nine positions over a glass: Vds=10V, W/L=25/25㎛, without passivation. Cross section FIB images of the TFT devices (a) at position 9 ;edge region (b) at position 7;center region.



(a)



(b)

Figure 3. (a) IGZO blanket film thickness map over a glass with the uniformity of 23.5%. Target thickness was 700Å (b) The threshold voltage map of TFT TEG devices with W/L=25/25㎛ where S/D was dry etched without passivation.

field effect mobility, sub-threshold swing (SS), V_{th}, and on/off current ratio over the glass were 11.7±0.6cm^2/(V·sec), 0.99±0.08V/dec, -1.2±4.4V, and >10^7, respectively. Standard deviation of V_{th} is a key indicator of the IGZO TFT's uniformity. Positions at 9, 6, and 3 show a large negative V_{th} shift compared to other positions. The mobility, V_{th}, and SS of position 9 were 10.3cm^2/(V·sec), -11.8V, and 1.19V/dec while those of center position 7 were 11.9cm^2/(V·sec), -0.9V, and 0.97V/dec, respectively. Cross sectional images of the TFTs, as shown in Fig.2 (b) and (c), indicate that position 9 has higher thickness (830Å) than position 7 (550Å). Although target thickness of IGZO was 700Å, standard deviation of IGZO channel thickness was 23.5%. Thickness variation of SiNx gate insulator was within 1%, therefore, the negative shift of V_{th}, reduction of field effective mobility and the increase of SS is attributed to the increase of IGZO channel thickness. Especially, threshold voltage shift between two regions is quite a large compared to other parameters. The thickness map of 260x360cm^2 IGZO blanket film is shown in Fig. 3(a). The thickness uniformity was 23.5% which is described by:

Uniformity (%)
= [{(Max THK)-(Min THK)}/{(Max THK)+(Min THK)}]x100.

The V_{th} map of TFTs well matches with the thickness map as shown in Fig.3 (b) macroscopically. Mobility map showed similar trend (not shown here). In the previous report, S/D contact effect which is closely related with parasitic resistance (R_p) decreased apparent field effective mobility, V_{th} and increased SS with decrease of channel length [4-5]. GIZO TFTs also show the short channel effect (not shown here). Interestingly, the effect of channel thickness is similar to that of channel length on the TFT parameters. Parasitic resistance (R_p) includes not only S/D interface resistance but also bulk effect and is believed to be associated with threshold voltage shift especially. Therefore, to achieve small variation of V_{th}, the thickness uniformity of IGZO layer should be controlled within some range before passivation step. Table 2 shows the TFT characteristics at W/L= 25/4µm according to S/D etching technology. Average mobility and V_{th} of S/D wet etched TFTs are

Table 2. TFT characteristics of devices at W/L= 25/4µm over a glass according to S/D Mo etching methodology before passivation.

IGZO TFT	Mobility (cm^2/V-s)	Threshold Voltage (V)	Sub-threshold Swing(SS)
S/D wet	8.04±1.04	-6.65±3.14	1.0±0.10
S/D dry	5.6±0.98	-9.9±2.20	1.09±0.16

higher than those of dry etched TFTs. The result can be attributed to the creation of traps due to the plasma damage to the IGZO back channel during the S/D dry etching. Sub-threshold swing was almost the same, which is related with the IGZO/gate insulator interface. V_{th} map processed with S/D wet etching showed the similar contour to dry etched glass.

Fig. 4 shows I_d-V_{gs} transfer curve of TFTs after SiOx passivation deposition and annealing process at 25 ℃ in air. Surprisingly, a controlled SiOx deposition and subsequent annealing process reduced long range order of V_{th} variation as shown in Table 3. Although there were variations of V_{th} which were dependent on IGZO thickness after S/D patterning, SiOx passivation and a subsequent annealing process compensated the effect. Compared to TFTs without SiOx passivation step, field effective mobility was reduced but V_{th} was increased. In terms of the mobility, the trend was similar to the previously reported one however, the V_{th} shift showed the opposite tendency [6]. The annealing process caused increased field effective mobility and decreased V_{th} in our experiments. For driving TFT- LCDs, a large negative V_{th} shift is not beneficial. V_{th} shift in the positive direction can be attained by changing SiOx passivation process parameters as shown Fig.5. PVX-2 was made with higher oxygen process conditions than PVX-1. In the back channel region of the IGZO channel layer, etching or plasma damage induced conduction electron accumulation but oxygen supply by passivation reduced carrier densities and accordingly V_{th} shift in the positive direction. Fig. 6 shows the display image of a 15-inch LCD panel using IGZO oxide TFTs. The specification of the LCD display is summarized in Table.4.

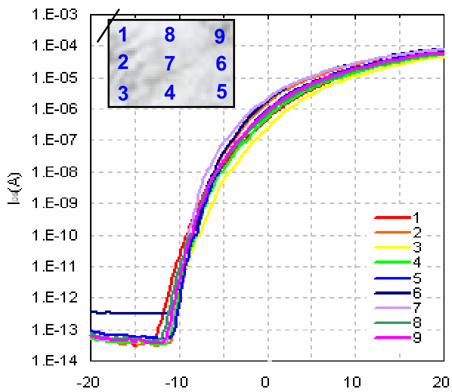


Figure 4. Transfer curves of IGZO (700Å) TFTs at 9 positions over a glass: V_{ds}=10V, W/L= 25/4µm, with SiOx passivation where S/D was wet etched.

Table 3. TFT characteristics of devices over a glass after SiOx passivation deposition and post-annealing process at 250℃; W/L = 25/4µm, V_{ds}=10V, and S/D Mo was wet etched.

IGZO TFT	Mobility (cm^2/V-s)	Threshold Voltage (V)	Sub-threshold Swing (SS)
S/D wet	4.20±0.40	-1.30±1.40	0.96±0.10

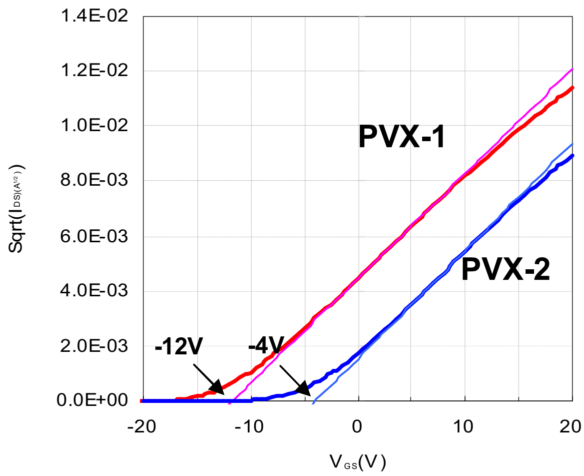


Fig.5. Representative threshold voltages of IGZO TFTs according to SiOx passivation process conditions (PVX-1, PVX-2) in which the same post-annealing condition was applied

4. Conclusion

The main steps affecting process development of IGZO TFTs for high quality and large area AMLCD applications in terms of V_{th} and its uniformity using

Fig.6. 15-inch XGA LCD display (left) driven by IGZO TFT array

Table 4. IGZO TFT-LCD display specification

Item	Specification
Size	15.0 inch (diagonal)
Resolution	1,024x768 (x 3 RGB:XGA)
Aperture ratio	54.52%
LC mode	TN (Twisted Nematic)
TFT W/L (μm)	29.5/4 (μm)

back channel etched (BCE) structure were analyzed. IGZO thickness, S/D etching conditions, passivation and annealing processes played a key role in improving V_{th} uniformity. SiOx passivation and post-annealing processes were more effective for minimization of long range V_{th} standard deviation than the control of IGZO thickness. Optimized SiOx passivation procedure caused V_{th} shift in the positive direction. Finally, we developed the world's largest (15-inch) XGA AMLCD panel using IGZO TFTs (W/L= 29.5/4μm) with a field effective mobility of 4.2±0.4 cm^2/V-s, V_{th} of -1.3±1.4V, and sub-threshold swing (SS) of 0.96±0.10 V/dec.

5. References

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