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Optimized Design of Low Voltage High Current Ferrite Planar Inductor for 10 MHz On-chip Power Module

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1. Introduction

The input voltage of the base-band processor is lowered to avoid overheat of finer conduction line [1], which is the same trend for other CPUs (Central Processing Unit). At present, around 1 V is supplied to CPU, therefore, current is increased up to several amperes in a smart phone. In order to achieve small ripple voltage, the integrated and miniaturized on-chip power module has been intensively studied. On the other hand, an increase in switching frequency decreases inductance (L) and capacitance (C) in the power circuit, resulting in size reduction and integration of passive components. The switching frequency of commercial DC-DC converter has already been increased up to 5 MHz [2]. A high Q inductor is an essential component for high efficiency DC-DC converters. Therefore, a DC-DC converter with an air-core chip inductor was proposed to achieve high Q at high frequency. However, the air-core inductor Q is still below 20 in the 10 ~ 100 MHz range.

In this work, we proposed the 1 ~ 2 W buck-type one-chip power module having 0.25 V and 5 A out put as shown in Fig. 1. And then, the optimized design parameters of a ferrite planar inductor, which has high Q over 50 at 10 ~ 100 MHz, for use in the one-chip power module were reported. We used DOE (Design of Experiment; one of the common six-sigma tools) method to optimize space and thickness of copper coil and thickness and permeability of ferrite film.

2. Design parameters and DOE

A UA-C type spiral inductor design is used for DOE because of its high L/area property. Copper coil with area of 5 x 5 mm^2 was designed on a 600 μm thick Si substrate. Copper coil thickness is in the range of 50 ~ 100 μm and is assigned as an X factor of the DOE. These thicknesses are greater than double the skin depth at 10 MHz. Cross-sectional coil area was designed 0.025 mm^2 to withstand joule heating by maximum 5 A rated current. This value is determined from references of high current inductors. Therefore, line width of Cu coil is fixed at 500 μm. Coil spacing is assigned as an X factor of the DOE and is in the range of 2 ~ 500 μm. In principal, inductor needs inductance of 125 nH at 10 MHz. This is calculated by Wong's critical inductance equation [3]. Accordingly, 2.5 turns of spiral coil was determined. In order to optimize the design parameters, a 4 Xs 3 Ys 3 level DOE is carried out. The 25 X-Y conditions were determined by $2n + 2^n + 1$ (n = number of Xs) as a central composite design of DOE. The Ys of 25 inductors with different Xs were simulated and analyzed. The DOE-Pro software, commercial package, is used for this analysis.

3. Results and discussion

It was found that a high Q inductor requires 100 ~ 300 μm thick ferrite film and high permeability.

From the DOE results, Y's of L 125 nH, Q 197.5 and f_r 16.3 MHz are calculated from X's of A 127 μm, B 67.8 μm, C 130.3 μm and D 156.5. Actually, there are some difficulties to fabricate the 130.3 μm thick ferrite film below 400 °C. However, it is possible to fix C at 3 μm for consideration by general vacuum deposition system process capability to obtain Y's of L 66.1 nH, Q 74.6, f_r 632.4 MHz for X's of A 210 μm, B 64 μm, C 3 μm, and D 200. These calculations are verified by re-simulation with the same X's conditions. Its deviations are -9.1% in L, 2.8% in Q and 4.1% in f_r, therefore, it is found to have confidence levels of roughly over 90% for L and 95% for Q and f_r . However, tan δ = 0 is assumed in all the above cases. The quality factor Q will be decreased 50% at tan δ = 0.01 and 70% at 0.02 from the calculation. So, a tan δ < 0.02 ferrite film is strongly recommended to get Q > 50.

4. Conclusion

Optimized design parameters for a high Q, high current ferrite inductor for 10 MHz switching, 1~2 W on-chip power module for the baseband chip of smart phone were proposed and demonstrated. In this work, three regression equations on the Ys were derived by DOE. Four Xs were optimized using these equations. From results, we have successfully designed a 5 x 5 mm^2 ferrite inductor which has Q above 50 at 10 MHz. The following design parameters, 2.5 turns of coil, coil line width of 500 μm, Cu coil thickness of 64 μm, loss tan δ < 0.02, ferrite thickness > 3 μm, and permeability > 157 were determined to achieve an inductor with Q factor over 50 at 10 MHz. In addition, it was found that the optimized value of coil spacing is dependent on the ferrite thickness. Therefore, recalculations by regression equations are recommended for another ferrite thickness.

5. References

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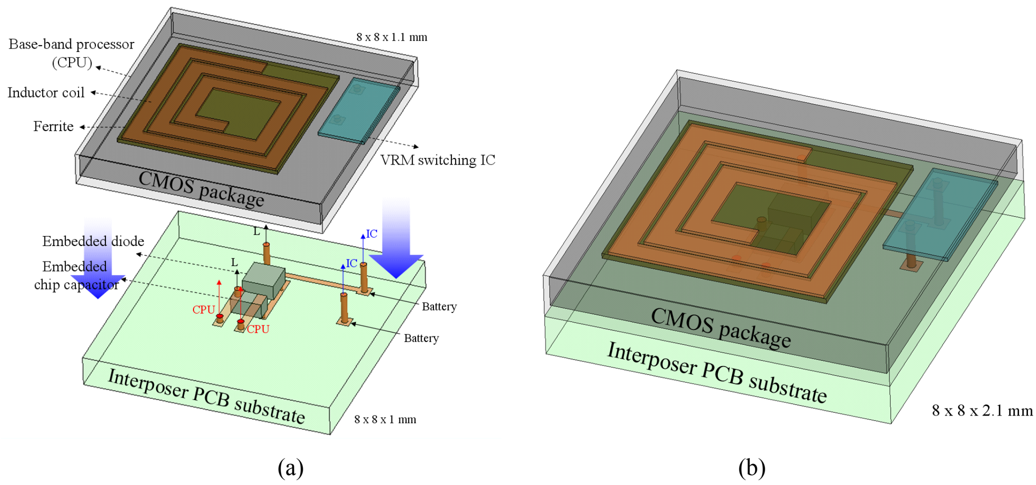

Fig. 1. Proposed one-chip power module: (a) CMOS package and interposer PCB substrate, and (b) assembled module.