

# Memory Characteristics Of Silicon Nanocrystal Dot Memory Device With Er-Silicide Source/Drain Structure

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Nonvolatile floating gate memories(NFGM) have attracted attention since modern nanotechnology enables us to fabricate very small structures. NFGM is candidate for future memory because of its advantages over conventional flash memory; high-speed write/erase time, small size, good scalability, and low operating voltage. But, as the feature size conventional NFGM with metal-oxide-semiconductor field-effect-transistor(MOSFET) structure has been scaled down to several deca-nanometer regime, the technologies face many challenged. For scaling down MOSFET, the formation of an ultra shallow source/drain(S/D) junction is essential and uneasy. This obstacle can be overcome with Schottky barrier (SB) MOSFETs instead of ion doping method.

So, We have fabricated the nonvolatile floating gate memory device with Si-nanocrystal based on Schottky Barrier S/D Structure. Moreover, the structure is quite simple and the ultra shallow junction can formed easily and accurately. Erbium is chosen as the S/D metal of n-type Schottky barrier MOSFETs, because of its low schottky barrier height for electron. The fabrication processes began with the  $\langle 100 \rangle$  p-type silicon-on-insulator(SOI) wafer (14~24  $\Omega\text{cm}$ ). The active area of SB memory device is first patterned on a planar SOI substrate. Following patterned active area, A thin tunnel oxide (~5 nm) was grown by dry oxidation and then a layer of uniform Si-nanocrystal dots with a FWHM of  $6\pm 1\text{nm}$  and a density of  $7\times 10^{11}\text{ cm}^{-2}$  was deposited by a digital gas-feeding method in the LPCVD process. And the control oxide was deposited 30 nm thick  $\text{SiO}_2$  using LPCVD at 400  $^\circ\text{C}$ , and the gate electrode was deposited highly phosphorus doped n-type polycrystalline silicon. After gate etching, 140nm thick gate sidewall spacer was formed by LPCVD. Then etching of gate sidewall spacer, Erbium silicide in the source/drain was grown by RTA process after Erbium was sputtered and non-reacted erbium removed by wet etch in Sulphuric-acid hydrogen Peroxide Mixed (SPM) solution. We achieved the memory window of NC is 4.5V. Program/erase time was 500ms/1s for 18V/-16V respectively.