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The effect of electrical stress on the leakage current of polycrystalline silicon transistors

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In this paper, we report the effect of electrical stress on the leakage current of polycrystalline silicon transistors. The self-aligned top gate thin-film transistors (TFTs) was fabricated by amorphous-Si film of 100nm thickness, silicon oxide of 100nm thickness and MoW gate layer of 300nm thickness (Fig. 1 (a)). Polycrystalline silicon transistor was fabricated by metal induced lateral crystallization (MILC). 200nm thick Ni film was deposited on amorphous silicon transistor and then ion doping was preformed by ion mass doping system using B_2H_6 diluted with H_2 gas. The transistor sample were annealed at 550°C for 4h and measured the crystallized length with optical microscope. The transfer characteristics and stress effects were measured at room temperature with a Keithley 4200-SCS system. The leakage current characteristics of TFTs can be effectively decreased after the electrical bias stressing as shown in Fig. 1 (b).

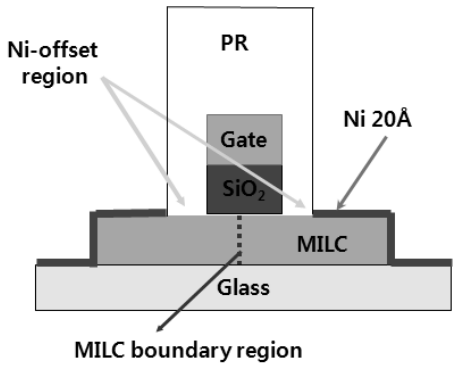

Fig. 1 (a) A schematic of the self-aligned to top gate TFT structure on glass

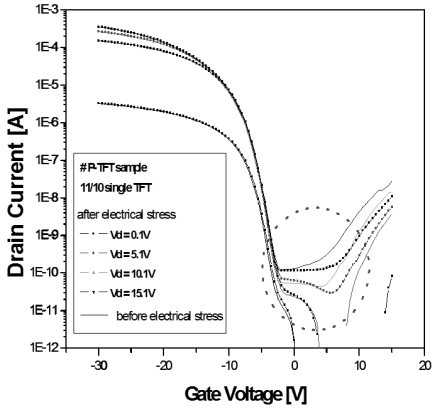

Fig. 1 (b) Transfer characteristics for before bias stressing and after different stressing voltage