SW1-08

The failure origin of PRAM device based on Ge₂Sb₂Te₅ with the oxygen impurity

 $\underline{\mathbf{SU2}}^1$, 신현준 1 , 홍성훈 2 , 황재연 2 , 배병주 2 , 이헌 2

¹포항가속기연구소 빔라인부, ²고려대학교 신소재공학과

Phase-change random access memory (PRAM) has been attracted as the most promising non-volatile memory for next generation. PRAM stores the digital data by reversibly changing resistance of phase-change material, which has a huge difference in resistivity between the amorphous and crystalline phases. As a phase-change medium for PRAM, Ge₂Sb₂Te₅ (GST) has been widely used due to its large sensing signal margin and fast programming speed. PRAM has lots of merits such as low operation voltage, high speed operation, good data retention, high scalability. However, PRAM device is not yet commercialized mainly because of its poor reliability. Thus, understanding the failure mechanism of the PRAM device is much needed. Here, by using the scanning photoelectron microscopy (SPEM) with synchrotron radiation we for the first time investigated the failure mechanism of PRAM devices based on the GST system having oxygen as an impurity. To this end, a lateral-type GST based PRAM device was fabricated. After repeated switching, under severe switching conditions, the PRAM device failed to the SET state and stuck to low resistance state and did not get back to high resistance state on the RESET. The SPEM images and spectra of the SET failed device showed that many of Sb atoms and part of Ge atoms, which were incorporated with oxygen (chemically oxide), respectively, diffused towards the region far away from the Mo electrodes. Meanwhile, most of the Te atoms, incorporated with oxygen, remained in the middle part of the GST. The analysis suggests that the reason of the device failure is mainly the out-diffusion of Sb atoms with oxygen through the SET and RESET processing. The remaining GST system with less Sb oxide has been suggested to be more metallic than the GST with more Sb oxide and the generation of more metallic path between the Mo electrodes is suggested to be the cause of failure of the phase transition by SET and RESET.