Low voltage operated top gated polymer thin film transistors with a high capacitance polymer dielectric

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Abstract

Low voltage operated top gated polymer transistors were fabricated with a high permittivity polymer, P(VDF-TrFE) and F8T2 as a gate dielectric and semiconducting layer, respectively. The operating voltage of transistors was effectively reduced under -10 V and typical threshold voltages were as low as -1 ~ -4 V with the reasonable charge carrier mobility of 10^{-3} cm^2/Vs for the amorphous polymer. The large hysteresis in transfer curve was improved effectively by annealing at low temperature.

1. Introduction

Organic thin film transistors (OTFTs) fabricated by solution process are emerging devices being able to realize various flexible and light weight electronics via a cost-effective method [1]. Since OTFTs are expected to apply in various mobile electronic devices, a low power consumption of circuits including OTFTs is needed. The operating voltage of OTFTs depends on the dielectrics constant and thickness of gate dielectrics. Gate dielectrics with a high permittivity have a benefit to reduce operating voltage of OTFTs effectively without thickness reduction which can degrade device reliability and yield via an electrical shorting through gate dielectrics or a large gate leakage.

Here we demonstrate low voltage operated top gated polymer transistors with a high permittivity polymer dielectric, poly (vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)]. Amorphous conjugated polymer, poly(9,9-dioctylfuorene-*co*-bithiophene) (F8T2) was used. Our top gated polymer transistors showed a very low threshold voltage (Vth) around -1 ~ -4 V with the reasonable charge carrier mobility of 10^{-3} cm^2/Vs for the amorphous polymer due to a high permittivity of P(VDF-TrFE) (C_i~10) [2]. Hysteresis behavior of transfer curve in F8T2 transistors was effectively reduced via annealing at a mild temperature which is lower than the crystallization temperature of P(VDF-TrFE) film.

2. Experimental

Corning 7059 glass slides were used as substrates after cleaning sequentially in an ultrasonic bath with deionised water, acetone and isopropanol for 10 minutes each. The gold patterns for source and drain electrode were fabricated using conventional lift-off photolithography. The semiconducting polymer, poly (9,9-dioctylfuorene-*co*-bithiophene) (F8T2) (American dye source) was dissolved in anhydrous xylene (0.7 wt.%) and filtered with PTFE syringe filter to remove impurities. Films were annealed at 100 ^oC for 30 min to remove the solvent after spinning (2000 rpm, 1 min) in a glove box with low oxygen and moisture level (< 5 ppm). For thin polymer dielectrics, organic ferroelectric P(VDF-TrFE) film was deposited by the spin-coating. P(VDF-TrFE) copolymer in a molar ratio of 70/30 was obtained from Solvay SA and used as-received. P(VDF-TrFE) powder was dissolved in *N*,*N*-dimethylformamide (DMF) at a concentration of 3 wt.%, and the solution was then filtered by a 0.2-μm PTFE syringe filter. A 3 wt.% diluted solution was spun on substrates at a spin rate of 2000 rpm for 10 s and then dried on a hot plate at 70 °C for 5 min. Final

film thickness was controlled by carefully monitoring the spinning speed and time. Finally, the films were annealed at 100°C for 30 min under air to remove residual solvent. Top-gate transistors were completed by formation of a gate electrode via evaporation of thin Au or Al films through a shadow mask [Fig 1]. The electrical characteristics were measured with HP4156A semiconductor parameter analyzer and HP 4194A impedance analyzer in air atmosphere. Ferroelectric properties of the films were examined by a precision LC materials analyzer (Radiant Technologies, Inc., New Mexico). The transistors parameters such as charge carrier mobility were calculated in the saturation or linear regime using the standard formalism for field-effect transistors [3].

3. Results and discussion

Figure 1 shows schematic diagram of top gated F8T2 polymer transistors with P(VDF-TrFE) gate dielectrics. OTFT with P(VDF-TrFE) typically showed a large hysteresis in transfer curve by alignment of permanent dipole induced by thermal annealing. The reversible large hysteresis is key characteristic for organic ferroelectric memory devices and but is not good for OTFTs and circuit with them. Therefore, P(VDF-TrFE) films were annealed at a relatively low temperature (100°C) due to avoid large electrical hysteresis via a crystallization of the ferroelectric polymer (>150°C). Nevertheless, the P(VDF-TrFE) films showed a hysteresis behavior at some extent as shown in capacitance versus voltage characteristics.

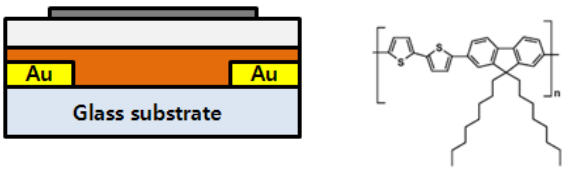

Fig. 1. Schematic diagram of a top-gated polymer transistor and molecular structure of F8T2.

Metal-insulator-metal diode was fabricated to measure hysteresis behavior of P(VDF-TrFE) films. P(VDF-TrFE) films annealed at 100°C showed a small capacitance hysteresis as shown in Figure 2. The AFM data of the film showed crystalline domain with a few hundred nanometer size even annealed at such a low temperature. We reduced the hysteresis via a lower temperature annealing or blending with amorphous insulating polymer such as poly(methyl methacrylate) (PMMA). The main results will be discussed at the conference site.

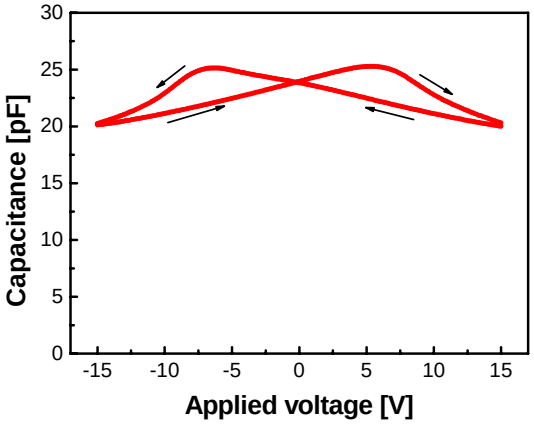

Fig. 2. Capacitance versus voltage curve of Ni/P(VDF-TrFE)/Ni, metal-insulator-metal diode.

Figure 3 and 4 show transfer and output characteristics of top gate F8T2 based polymer transistors with P(VDF-TrFE), respectively. The transistors showed a very low operating voltage due to a relatively high permittivity P(VDF-TrFE) (C_i=8 ~ 8.5) of comparing with other OTFTs with conventional polymer dielectrics. The measured Vth was as low as -1 ~ -4 V and charge carrier mobility was 10^{-3} cm^2/Vs which is comparable with previous reports with conventional polymer dielectrics such as PMMA, PS, and PVP.[] However, a some extent of hysteresis in transfer curve was observed due to ferroelectric properties of P(VDF-TrFE) [Fig 3]. This behavior is due to crystallization of the polymer and consistent with capacitance versus voltage characteristics and AFM results. We obtained improved results without distinguishable hysteresis in transfer curve via low temperature annealing at 70°C or blending with PMMA to disturb crystallization of P(VDF-TrFE) film. The results will be discussed at the conference.

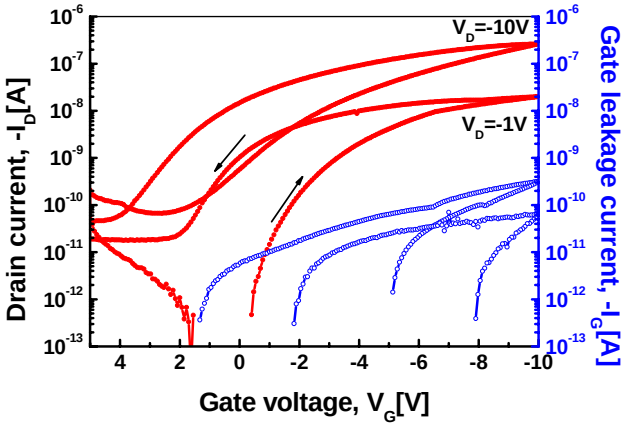

Fig. 3. Transfer curves of top gated F8T2/P(VDF-TrFE) transistors .

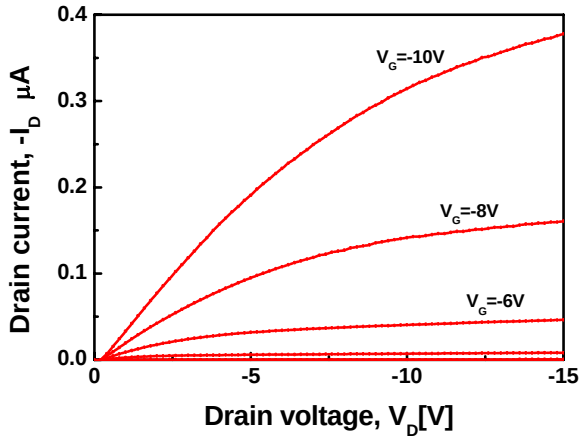

Fig. 4. Output curves of top gated F8T2/P(VDF-TrFE) transistors .

4. Summary

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We have demonstrated low voltage operated top gate polymer transistors with a ferroelectric polymer P(VDF-TrFE). Our F8T2 polymer transistors showed a low operating voltage under -10 V and typical threshold voltages were as low as -1 ~ -4 V with the reasonable charge carrier mobility of 10^{-3} cm^2/Vs for the amorphous polymer. The annealing temperature of this dielectric is a relatively low which is suitable to plastic substrate. We expect the high permittivity polymer is promising materials for solution processed organic or flexible integrated circuits with a low power consumption.

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5. References

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