Direct deposition technique for poly-SiGe thin film achieving a mobility exceeding 20 cm^2/Vs with ~30 nm thick bottom-gate TFTs

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Abstract

High quality poly-SiGe thin films were prepared on 6-inch substrates using Reactive-thermal CVD with Si_2H_6 and GeF_4 around at 500 °C directly. Its thickness uniformity was ~ 3% on the entire substrate area. N-channel mobility of ~30 nm thick bottom-gate TFTs exceeded 20 cm^2/Vs without any further crystallization.

1. Introduction

Recently, thin film transistor (TFT) materials having higher mobility over that of a-Si:H TFT, e.g., 5 to 10 cm^2/Vs, is demanded to fabricate active matrices for high definition large-size liquid crystal TVs operated at a higher frequency and for organic electroluminescence TVs.

The excimer laser annealing of amorphous silicon technique has applied to fabricate high quality poly-Si thin films for small-size mobile displays including organic EL displays already. However, it is very hard to apply this technique to the large-size active matrices because of high installation and running costs and limited substrate-size available for the excimer laser annealing.

Poly-Si thin film deposited by a CVD process directly on glass substrates is a good candidate for such applications, because the CVD process has high potential to deposit uniform poly-Si thin films on large-size glass substrate in a low-cost, in addition to technical continuity of Si-based technologies in the display industry. However, no CVD technique has been established to fabricate device-grade poly-Si thin films yet.

Since 1994, we have challenged to establish a CVD technique that allows us to deposit device-grade poly-Si and poly-SiGe films directly at temperatures lower than 500°C, where inexpensive glass substrates are available, including Reactive Thermal Chemical Vapor Deposition (*RT-CVD*) techniques, in which the chemical reactions of source gases, i.e., Si_2H_6 and GeF_4 or F_2 allow us deposit the films [1-5]. In this CVD technique, the chemical reaction, i.e. redox reactions in a set of the source materials is featured to promote their decomposition and crystal growth at temperatures lower than their pyrolytic temperatures as shown in Fig.1 [5].

In order to demonstrate their high crystallinity, we have fabricated bottom-gate TFTs [2-4], which requires high crystallinity at

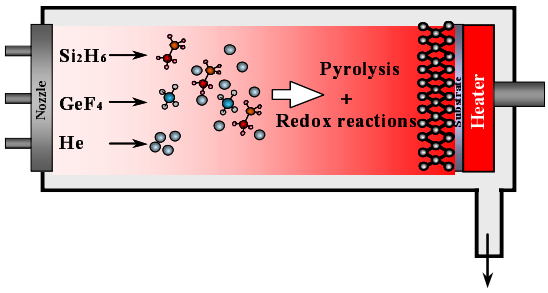

Fig. 1. Concept image of reactive thermal CVD of Si_2H_6 and GeF_4 system

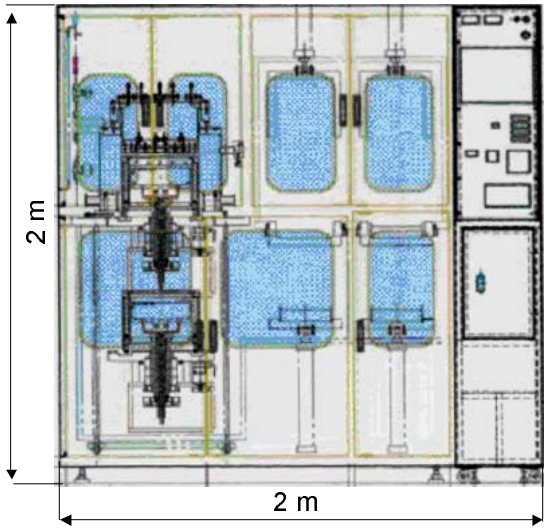

Fig. 2. Image of the up-scaled CVD where 6-inch substrate can be loaded.

an early stage of the film growth, because the channel region is formed at the interface between a gate material and a semiconductor thin film.

In this study, we installed a cold-wall type of large-reactor where 6-inch substrate can be loaded, to investigate the feasibility of scaling up low-temperature growth of poly-SiGe by a reactive thermal CVD technique, as shown in Fig.2. Optimization of growth conditions and the deposition system including a gas mixing system, a substrate heating method and a structure of showerhead-type of gas nozzle, were undertaken to obtain uniform and high crystallinity poly-SiGe films on the entire area of 6-inch substrates.

With very thin poly-SiGe films of ~30nm, we fabricated bottom-gate TFTs and evaluated their device performance.

2. Experimental

The up-scaled CVD is a cold-wall type reactor, where 6-inch wafer can be loaded as shown in Fig 2. It is a 2 x 2 x 1.5 m in size and consists of a main chamber and two robot arm rooms to keep a high level clean environment. The substrates used in present study were quartz and 300 nm oxidized silicon wafer whose size was all 6-inch.

Temperature and total pressure were varied from 450 to 550 °C and from 1 to 7 torr,

Fig. 3. **The surface image of Poly-SiGe thin film of 500 nm prepared on the 6-inch quartz at 520 °C.**

respectively. We kept a high gas flow ratio of Si_2H_6 to GeF_4 in order to deposit high Si content films over 95 at%: the gas flow rates of Si_2H_6 and GeF_4 were set for 1 and 0.06 ~ 0.2 sccm, respectively, while a flow rate of carrier gas of either He or Ar was set for 1000~4000 sccm. The film thickness and the average grain size were measured by scanning electron microscopy (SEM) and atomic force microscopy (AFM). To evaluate uniformity of thickness in the entire area of substrate, several points on the substrate were selected to measure. Transmission electron microscope (TEM) was used to examine the crystallographic and structural properties of the poly-$Si_{1-x}Ge_x$ films.

P-type and n-type bottom-gate TFTs were fabricated with poly-Si_xGe_{1-x} films of 30 nm prepared on thermally oxidized SiO_2 wafer. The thickness of the gate insulator, SiO_2 was 300nm. For n-type ohmic contact, P^+ ion were implanted at energy of 10 KeV and then annealed in nitrogen ambient at 600 °C for 1 hour and followed by hydrogenation with hot-wire techniques at 380 °C for 1 hr, for activation and defect passivation, respectively. After that an Al layer of 80 nm was resistively evaporated in vacuum and was patterned for electrodes. Each device was isolated by a dry etching of poly-Si films. Finally, hydrogenation was performed to ensure defects passivation by hot-wire technique at a substrate temperature of 200°C for n-type. The filament temperature was approximately 1100°C under a H_2 flow rate of 400sccm and 2Torr for 1hr.

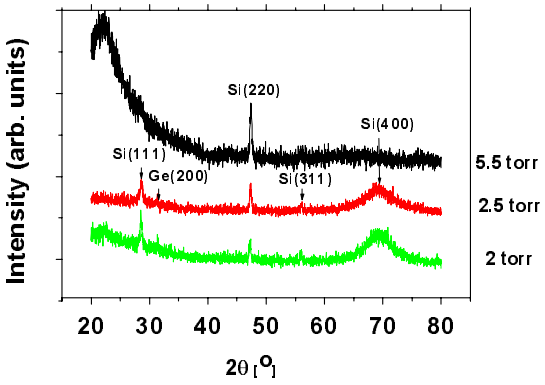

Fig. 4. XRD peaks of poly-SiGe film prepared at various process pressures of 2 ~ 5.5 torr.

3. Results and discussion

Fig. 3 shows the surface morphology of the poly-SiGe films on the 6-inch quartz substrate. Its thickness was around 500 nm. As shown, its uniformity of thickness was ~ 5%, which is estimated from the several points in the entire substrate. To achieve such a high uniformity, improvements of growth conditions and the CVD system such as the substrate heating method, gas mixing and showerhead structure was needed [6]. We found that how to control uniform introduction of source gases decides the uniformity of resulting films. For that we adopted a `Pre-Mixing System`, where mixture of three gases, i.e. Si_2H_6, GeF_4 and He was introduced uniformly into the chamber via a showerhead on which uniform gas outlet holes were designed [6]. Furthermore growth parameters were also optimised to achieve uniformity of the films: as we reported previously, where reaction of Si_2H_6 and GeF_4 occurs dominantly near the substrate regime or gas phase regime determines the growth mode and quality of films [4]; when premature gas phase reaction between Si_2H_6 and GeF_4 was suppressed, by-product decreased and etching reaction originated from GeF_4 is dominant, promoting crystallization; the parameters determining the reaction regime such as distance between showerhead and substrate,

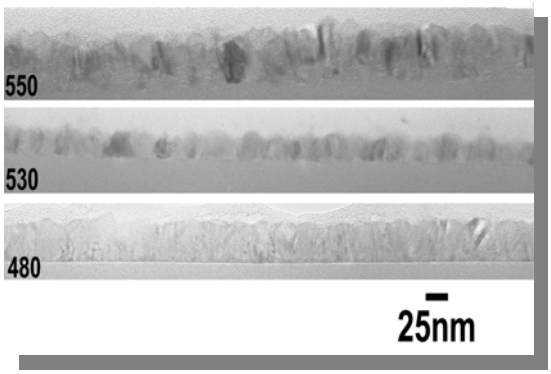

Fig. 5. TEM image of the SiGe films prepared on 6-inch SiO_2 substrate at various temperature of 480 ~ 550 °C

carrier gas and process pressure needs a careful control. Fig. 4 shows XRD peaks of poly-SiGe film prepared at various process pressures of 2 ~ 5.5 torr. Film prepared at 5.5 torr, (220) direction is dominant. (111),(200) and (311) for Si and (200) for Ge is shown for 2~2.5 torr. As process pressure was decreased, crystal orientation became random and Ge content was increased easily. It is plausible that the gas phase reaction is suppressed at lower pressures, and the surface reaction is activated because of more contribution of GeF4 on the surface, so it changes surface reaction. The total amount of Ge film prepared at 2.5 torr was ~ 6 %, estimated from X-ray photoelectron spectroscopy. Fig. 5 shows the TEM image of the SiGe films prepared on 6-inch SiO_2 substrate at various temperatures of 480 ~ 550 °C, whose thickness was around 30 nm. It is worth noting that in spite of such a thin film of 30 nm, all films shown the obvious crystallite growth from the initial stage of growth. Their crystallinity estimated from

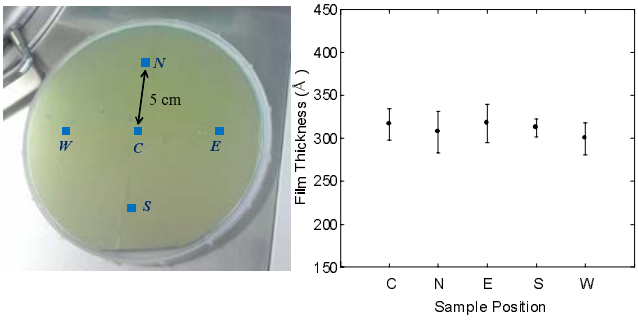

Fig. 6. The surface image of Poly-SiGe thin film of 30nm prepared on 6-inch SiO2 substrate at 520 ℃ and its uniformity.

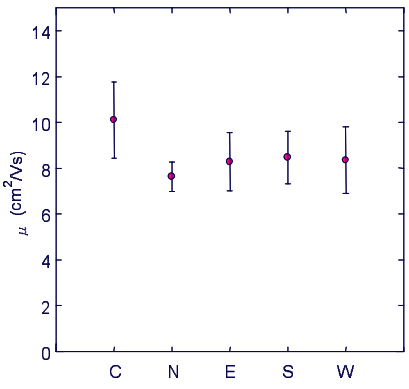

Fig. 7. The mobility uniformity of p-type 30 nm poly-SiGe bottom-gate TFT

Raman and ellipsometry was around 90 % and it is well coincident with the TEM images. In contrast, in conventional low-temperature CVDs including plasma-enhanced CVDs, 30 nm thick films are rich in amorphous tissue and exhibit poor crystallinity. As temperature was increased, the roughness of interface between poly-SiGe and SiO_2 and grain size were increased. Fig. 6 shows the surface image of the poly-SiGe film of ~30 nm prepared at 520 °C and its uniformity. Its thickness uniformity was within ~ 3%. Finally, we fabricated bottom-gate TFTs with this film. As shown in Fig. 7, we achieved a mobility of 8 ~ 10 cm^2/Vs and a V_{th} of ~ 32 V with p channel TFTs without any crystallization process, after an atomic hydrogen treatment for a defect passivation using a hot-wire apparatus. It is worth noting that its uniformity of not only thickness but also device performance is excellent. Fig. 8 shows the transfer characteristics of n-type bottom-gate TFT with 30 nm thick poly-SiGe thin film. An as-prepared film was hardly operated, but after post deposition passivation (PDP) at 380 °C for 1hr, its performance was drastically improved. Its mobility was ~15 cm^2/Vs, and improved further up to ~24 cm^2/Vs, after post metallization passivation (PMP) at 200 °C for 1hr.

4. Summary

High crystallinity and uniform poly-SiGe thin films were prepared on 6-inch glass substrates using *RT-CVD* with Si_2H_6 and GeF_4 around at 500 °C directly. Its thickness

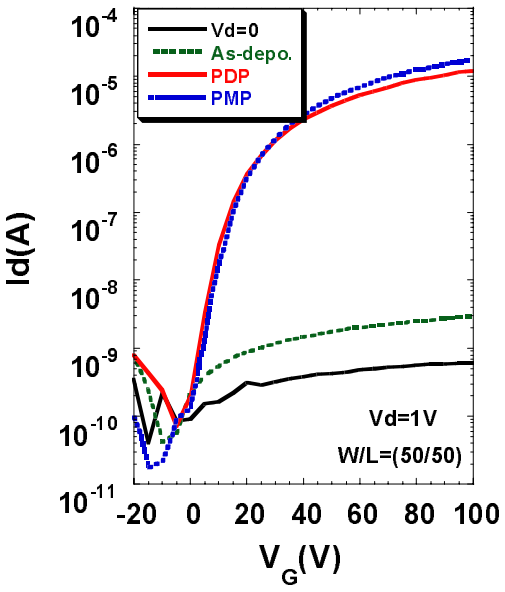

Fig. 8. Transfer characteristics of n-type 30 nm poly-SiGe bottom-gate TFT

uniformity was ~ 3% on the entire substrate area. N-channel mobility of ~30 nm thick bottom-gate TFTs exceeded 20 cm^2/Vs without any further crystallization. We conclude that this technique can be a good candidate for industrial production of poly-Si backplanes for large-area displays in low cost.

5. References

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