Self sustained n-type memory transistor devices based on natural cellulose paper fibers

R. Martins*, P. Barquinha, L. Pereira, G. Gonçalves, I. Ferreira, E. Fortunato
Materials Science Dept, CENIMAT/I3N, FCT-UNL and CEMOP/UNINOVA, Campus de Caparica, 2829-516 Caparica, Portugal
Phone:+351212948525 E-mail: rm@uninova.pt

Keywords: hybrid memories, floating memory, floating TFT memory

(2 line spacing)

Abstract

Here we report the architecture for a non-volatile n-type memory paper field-effect transistor. The device is built using the hybrid integration of natural cellulose fibers (pine and eucalyptus fibers embedded in an ionic resin), which act simultaneously as substrate and gate dielectric, with amorphous GIZO and IZO oxides as gate and channel layers, respectively. This is complemented by the use of continuous patterned metal layers as source/drain electrodes.

1. Introduction

The aim of this work is to show that paper can be used as an electrically active part of devices, working simultaneously as substrate and dielectric in n-type field effect transistors that will exhibit memory effects, when proper treat [1, 2]. In these devices the channel and gate electrode are based in active and passive multicomponent amorphous oxides, such as GIZO [3] and IZO [4]. This opens a new field of applications for the natural cellulose fibers, the earth's major biopolymer [5], the lightest, cheapest and easiest recyclable known substrate, as demanding by the industry., opening a new era lighter efficient and reliable disposable electronic devices, the so-called paper-e, the green electronics of the future.

2. Experimental

The devices were processed at room temperature by rf sputtering technique The device structure is shown in fig. 1 and has been produced as described elsewhere [3]. One side of the paper is coated with rf sputtered amorphous GIZO (thicknesses below 50 nm), that acts as the active channel layer [3]. The other side of the paper is coated with high conductive IZO prepared by rf sputtering, to act as the gate electrode [2]. This is complemented by the use of patterned metal layers as source/drain electrodes, connecting all coated paper fibbers. Both the semiconductor and the source/drain regions were patterned using shadow masks. The memory devices were characterized in air, at room temperature and in the dark using a Cascade Microtech M150 microprobe station connected to a semiconductor parameter analyzer (Agilent 4155C). For the write-erase stress test a square wave was applied to the gate electrode through a Wavetek 395 synthesized arbitrary waveform generator. The capacitance per unit area and the dielectric constant of the paper was measured by C-V and spectroscopic impedance methods.

3. Results and discussion

The device structure is shown in fig. 1. The operation of the device relies on the ability of the paper fibers to exhibit spontaneous polarization and to accumulate an enormous number of charges due to its sponge-like structure. This leads to an enormous increase of the lateral area of the entire set of fibers that constitute the gate dielectric. Besides, to reduce leakage and recombination losses, this structure is coated with amorphous multicomponent oxides on both sides, to produce highly smooth surfaces [7]. The device structure is shown in fig. 1.

The operation of the memory device relies on the capacity of the paper fibers to accumulate an enormous number of charges due to the sponge-like structure of the matrix where they are randomly distributed.

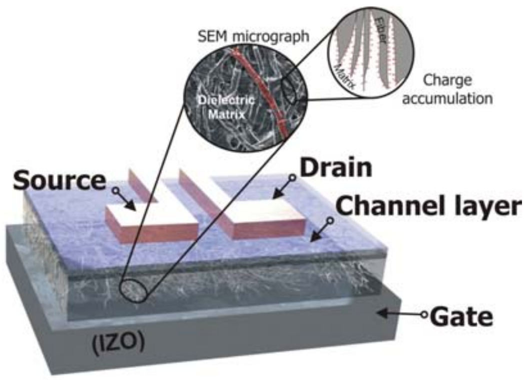
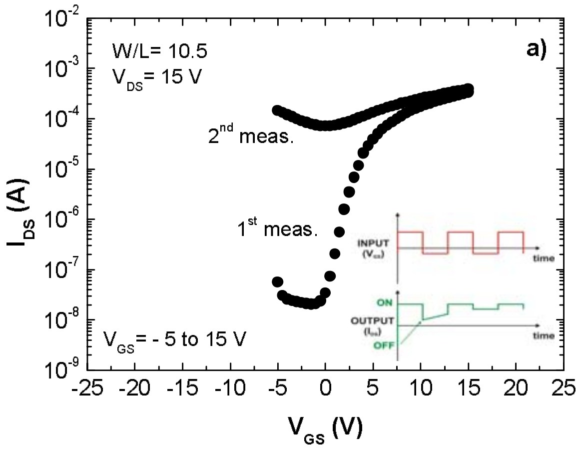


Fig. 1. Sketch of the device structure showing the different layers that constitute the final device. The magnified inset shows the fiber based dielectric structure and how carriers are accumulated along the fibers.

This leads to an enormous increase of the lateral area of the entire set of fibers that constitute the gate dielectric, when the fibers are properly prepared and the overall structure coated with the most suitable multicomponent amorphous oxides, to produce highly smooth surfaces, limiting so the device leakage current [7]. That is, the paper behaves like electrets [8] with the ability to retain permanent charges (mainly, ionic charges), function of the fibers and resin that constitute the paper structure. This leads to an overall enhancement of the device capacity to store charges. The electronic transfer characteristics of the processed devices are shown in figs. 2. Under the application of writing and erasing pulses on the gate (V_{GS}), large threshold voltages shift ($\cong$15 V) and on/off drain current ratio of 3×10^4 are obtained, with turn-on voltages (V_{on}) close to 0 Volts and saturation mobilities (μsat) above 45 $cm^2V^{-1}s^{-1}$.



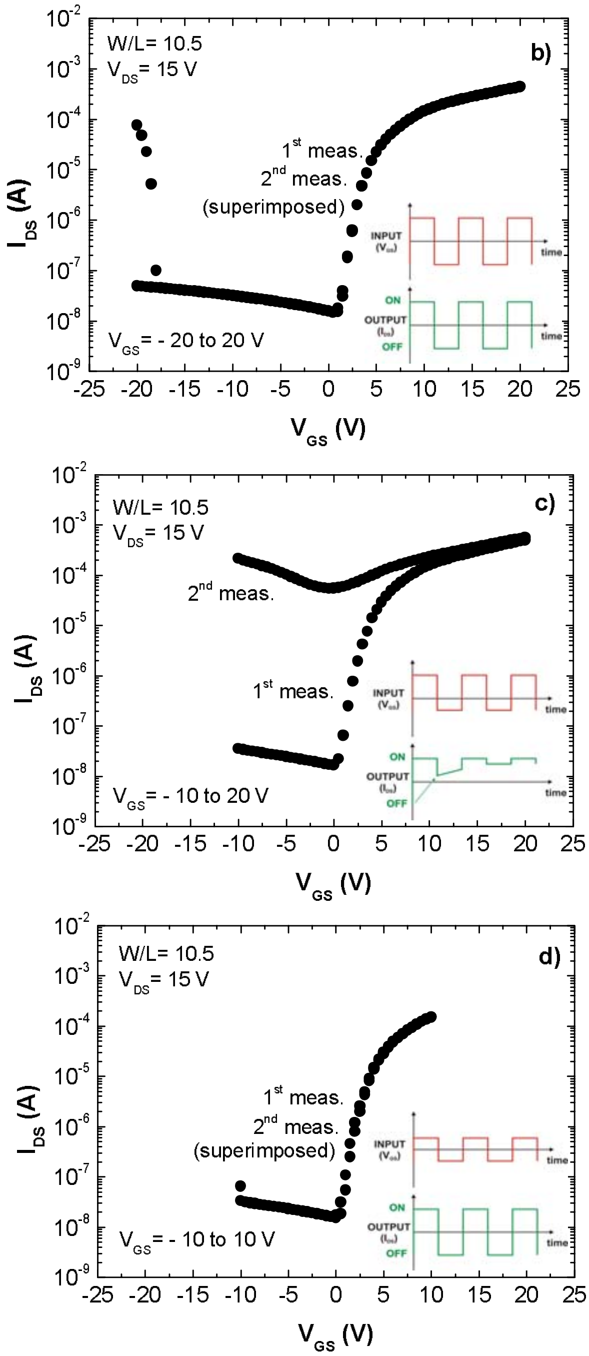


Fig. 2. Successive single sweep current-voltage transfer characteristics the memory paper for different V_{GS} ranges: a) -5 to 15 V; b) -20 to 20 V; c) -10 to 20 V; d) -10 Vto 10 V. The insets show schematics for input (V_{GS}) and output (I_{DS}) signals for each V_{GS} range.

The set of measurements performed show that the devices are highly stable. After sustaining more than 10^3 on-off cycles, the transfer characteristics of the devices remain the same, meaning that information can be written and erased many times without any apparent loss of performance. Apart from that, the devices show selectivity. If the absolute value of the off-state V_{GS} (erase) is smaller than the on-state V_{GS} (write), the carriers trapped/stored along the fibers (electrons + ions) are not fully removed and so they repeal the electrons accumulated in the channel region, avoiding so the pull-down of the drain saturation current (I_{DS}) towards its off-state value (see sketch in fig. 1 and results of the transfer characteristics in fig. 2), leading to a small difference between on and off states, i.e. to a low channel conductivity modulation and consequently to on/off ratio close to 1. That is, the on-state cannot be erased unless a symmetric V_{GS} to the one used for writing/store the information is used.

In order to be successfully used as memory, the devices should be able not only to write and erase information but also to store it [9]. Hence, to demonstrate the memory capacity, after changing the devices from off to the on-state (Write operation, accomplished by a single sweep transfer characteristic measurement), the gate electrode was opened and IDS evolution with the time monitored by more than 15 hours, keeping the drain voltage (V_{DS}) constant (15V), as shown in fig 3.

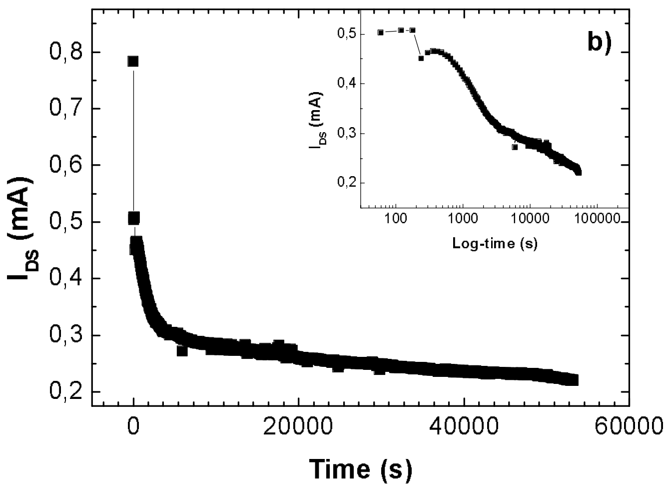


Fig. 3. Charge retention test, showing the evolution of IDS with time, after a single sweep transfer characteristic and after opening the gate electrode and keeping a constant VDS=15 V, for papers A (a) and B (b). The insets show semi-log representations of the main plots.

The inset in fig. 3 (semi-log scale) reveals an exponential dependence of the current as a function of the time, as expected [10]. The behavior of the drain current can be attributed to the role of the interface gap between the fibers filled with resin, within the active semiconductor region and so, charges are well distributed along the fibers.

After 8 months of the devices have been fabricated, their electronic performances do not change, showing that these flexible and disposable memories are highly environmental stable. In table 1 we present the performances of similar memory FET devices based on inorganic, organic and hybrid devices [11], as well as the ones of this work. The data depicted clearly show the high performance of the memory paper transistor, even at this early and non-optimized stage, when compared with all organic based memory devices [11]. The obtained results clear outpace those of memory FET based on organic polymers [12] and rival with the actual state of art concerning semiconductor oxides [13].

4. Summary

The compatibility of these low cost self sustained devices with large-scale/large-area conventional fabrication deposition techniques, together with their excellent electronic performance, such as stability, very low operating bias, high mobility and high charge retaining times, delineates a promising approach of using natural cellulose fiber paper on low cost high-performance flexible and disposable electronics [15, 16] like paper displays, smart labels, smart packaging, point-of-care systems for self analysis in bio-applications, RFID among others. This opens a new era away from silicon and related to low cost and disposable devices.

Acknowledgement

This work was supported by projects PTDC/CTM/23943/2006 and PTDC/EEA-ELC/ 64975/2006. The authors would like to thank Portuguese Science Foundation (FCT-MCTES) for the fellowships SFRH/BD/17970/2004 and SFRH/BD/27313/2006 given to two of the authors.

5. References

1. G. W. Scherer, *J. Am. Ceram. Soc.*, **73[11]**, p.3 (1990).
2. H. J. Kim and J. S. Im, *SID'05 Technical Digest*, Vol. **1**, p.401 (2005).
3. O.V. Mazurin and E.A. Porai-Koshits (eds.), Phase Separation in Glass, North-Holland, Amsterdam, p.21 (1984).
4. D.L. Eaten, Porous Glass Support Material, US Patent no. 904, 422(1975).
5. K. D. Hong, *IMID'06 Technical Digest*, p.877 (2006).