TF-P069

Carrier charging dynamics of multi-layered SiC nanocrystals embedded in SiO_2 dielectrics

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Nanocrystal memory devices have been required the materials to improve the memory properties by optimizing work function and band gap energy on the bases of Si device process. The silicon carbide (SiC) nanocrystal is the best way to deal with these problems, because it has an energy band gap of 2.0～3.2 eV and a work function of 4.0～4.5 eV, respectively. Especially, the multi-layer structure of SiC nanocrystal have possibility to enhance the efficiency of carrier charging effect of the nanocrystal memory device.

In this study, an activation energy for carrier charging and a current transient behavior in the multi-layered SiC nanocrystals embedded in SiO_2 dielectrics layer were characterized at various measuring temperatures. The multi-layered SiC nanocryals were fabricated on *p*-type and n^+-type Si wafers. The 4.5-nm-thick tunnel oxide layer was thermally grown by a dry oxidation process in an O_2 ambient furnace. Then, a SiC layer with a thickness of 12 nm was deposited on the tunnel oxide layer by using ultra-high vacuum (UHV) magnetron sputter. Also, an additional 50-nm-thick SiO_2 layer was deposited on the SiC layer. The first post-annealing process for SiC nanocrystal formation was carried out at 900°C for 3 min using a rapid thermal annealing system under ambient N_2. After this process, the 30-nm-thick control oxide layer was deposited by an UVH sputtering system. Finally, the Al metal gate with thickness of 150 nm was deposited to fabricate metal-oxide semiconductor by using thermal evaporator. The current-voltage and current transient measurements for MOS devices with SiC nanocrystals were carried out using HP-4156A precision semiconductor parameter analyzer and Agillent 81104A 80MHz pulse generator. We will discuss the carrier charging behavior of the multi-layered SiC nanocrystals embedded in SiO_2 dielectrics.