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Pentacene TFT properties with PVP on the SiO_2 as the gate insulator for low-voltage

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Pentacene thin-film transistors(TFTs) operating at low voltages with improve mobilities and leakage currents are successfully fabricated by the (poly-4-vinylphenol)PVP/SiO_2 gate dielectrics. The PVP film was deposited on the indium-tin-oxide(ITO) glass(sheet resistance~10Ω/□) substrate by the spin-coating. After it was deposited, SiO_2 was deposited by the thermal evaporator. From the electrical measurements, typical I-V characteristic and the field effect mobility of TFTs were observed. Using SiO_2 film, which has stabile thin film characteristics and relatively low leakage current. This double layer(PVP/SiO_2) can be improved electrical characteristic of OTFTs devices. Consequently, high leakage current of PVP gate dielectrics is a characteristic factor, which affects the performance of the OTFTs. The field-effect mobility is increased monotonically with the leakage current decrease.

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Inorganic high-k material related characteristics of organic thin film transistors

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The pentacene-based organic thin-film transistors(OTFTs) with a thin insulating inorganic Al_2O_3(high-k material) layer between the pentacene and source/drain electrodes were fabricated. Al_2O_3 as a gate insulator layer grown by atomic layer deposition(ALD). We showed the influence of surface roughness. Also inorganic high-k oxides as well as polymer dielectric were compared : Al_2O_3 deposited by ALD, polyvinyphenol(PVP) single layer or PVP/Al_2O_3 double layer. Atomic force microscopy(AFM) evidenced that surface roughness influence pentacene growth. Eventually, we point out the relationship between the grain size and the thin film transistor mobility. The results demonstrate that it is an effective method to improve the OTFT device characteristics by using a polymer/high-k oxide bi-layer dielectric configuration.