Implementation of Digital Control for Critical Conduction Mode Power Factor Correction Rectifier

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Abstract

In this paper, implementation of digital control for critical conduction mode power factor correction (PFC) rectifier is presented. Critical conduction mode is widely used in medium and low power conversion application due to its minimized MOSFET turn-on loss and diode reverse-recovery problem. However, it needs additional zero current detection circuit and maximum frequency limit to properly turn the MOSFET on and avoid the excessive switching loss in light load operation. This paper explains the digital IC implementation and verifies its operation with 200-W prototype PFC rectifier.

1. Introduction

Digital control of the switch mode power supply (SMPS) has been widely used recently thanks to its many advantages such as robustness to aging and environmental change, noise immunity, ease of re-programming and intelligent control [1]. The decreasing cost of the digital IC is also expanding the area of the digital control application. Power factor correction (PFC) rectifiers are especially suitable for digital control implementation because they require control loops with relatively low bandwidths than other applications [2]. In constant frequency operation, continuous-conduction-mode (CCM) PFC rectifier generally requires the current loop bandwidth below 10 kHz, and discontinuous-conduction-mode (DCM) PFC with single voltage loop needs the even lower bandwidth such as 10-20 Hz. These bandwidth guarantees sufficient calculation time for digital controller to update the duty cycle unless the switching frequency of the rectifier is excessively fast.

However, in critical conduction mode (CRM, also referred as boundary conduction mode, BCM, in literature) which is famous in medium and low power application, the switching frequency of the PFC rectifier varies in the half line cycle according to the line voltage and load. Specially, the rectifier may operate in very high switching frequency in high line voltage and light load condition, and this can cause severe switching loss in main switch and lack of calculation time for digital controller. Researches on CRM PFC have been reported to alleviate these problems. Limiting the maximum switching frequency to avoid the undesirable high frequency operation and obtain feasible operation of the CRM rectifier. Guaranteeing the minimum off-time of main switch is another method to indirectly regulate the operating frequency.

In this paper, digital implementation of CRM PFC rectifier with minimum off-time limit is presented. Operational analysis and practical implementation of the rectifier circuit is given. Experimental waveforms verify the feasibility of the implementation.

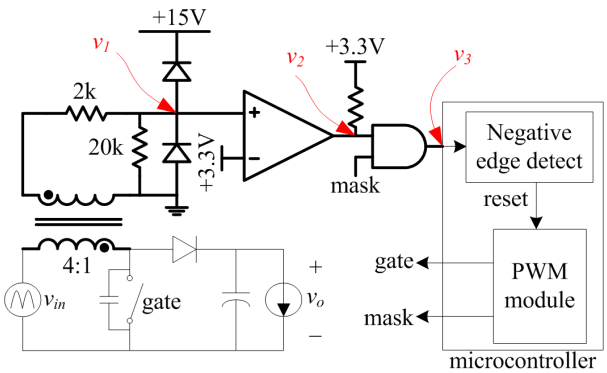

Fig. 1. Implementation of CRM PFC rectifier with digital control.

2. Implementation of Control Circuit

Fig. 1 shows the implementation of the CRM PFC rectifier. Zero current detection circuit of the rectifier is expressed in bold line. It consists of secondary winding of boost inductor, resistive voltage divider, clamping diodes, comparator, and AND logic element. The circuit detects the minimum or zero drain-source voltage of the main switch by sensing inductor voltage to

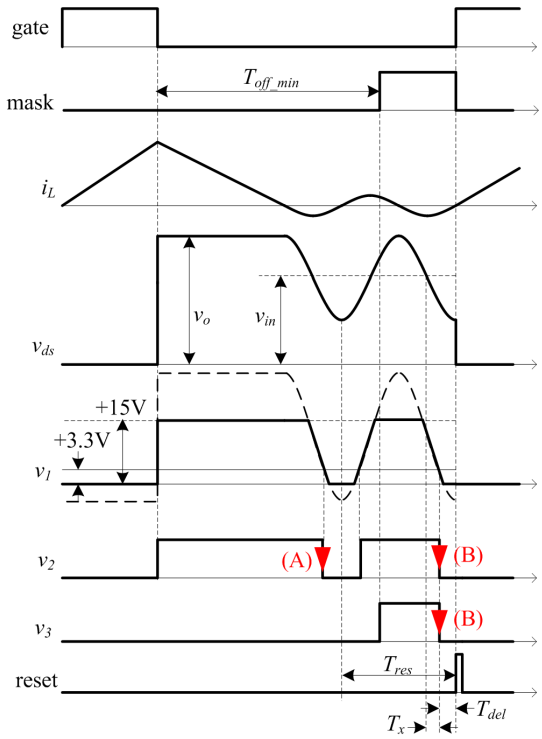

Fig. 2. Operational waveforms of zero current detection circuit.

Table I. Parameters of Prototype Rectifier Shown in Fig. 1

Parameter	Value/Part name
Main switch (R_{ds_on}, C_{oss})	IRF840 (0.75Ω, 130pF)
Output diode	MUR860
Clamping diodes	MBR0520CT
Comparator	LM2903
AND logic	74HC08
microcontroller	dsPIC33FJ16GS502
L	330uH
v_o	390VDC
v_{in}	200-240VAC

minimize the switching loss. The sequence of sensing is by following order: the voltage across the inductor is scaled, clamped and input to the positive terminal of the analog comparator such as v_1. Comparator output, v_2, and the mask signal from microcontroller is ANDed and the microcontroller detects the negative edge of the AND logic output, v_3. When the edge of v_3 is detected, an interrupt service routine is executed inside the microcontroller to reset the PWM period and initiate the next switching cycle. Mask signal generated by the PWM module in microcontroller is designed to be asserted when the on-time of the main switch is over and minimum off-time, $T_{off\text{-}min}$, is elapsed.

Operational waveforms are shown in Fig. 2, in which i_L and v_{ds} are inductor current and drain-source voltage of main switch. The mask signal limits the maximum operating frequency indirectly by guaranteeing the minimum off-time. If the negative edge of v_3 occurs before $T_{off\text{-}min}$ elapses, the edge is ignored as indicated by (A) in Fig. 2. After $T_{off\text{-}min}$ is elapsed and the other edge is detected as (B) in Fig 2, timer value in PWM period is reset after a certain delay. The delay time interval, T_{del}, is defined in (1):

$$T_{del} = \frac{T_{res}}{4} - T_x = \frac{\pi\sqrt{LC_{oss}}}{2} - T_x, \quad (1)$$

where L, C_{oss}, and T_{res} are boost inductance, parasitic output capacitance of the main switch, and their resonant period respectively. T_x in (1) indicates the time between the resonant point and effective negative edge of v_3.

Single voltage loop with 10-Hz bandwidth is implemented in the microcontroller. The loop calculates and updates the on-time of the switch. The off-time is not calculated but *interrupted* by reset signal. When the interrupt occurs, the gate and mask signals are reset to active-high and active-low respectively.

3. Experimental Results

To realize the operation, a 200-W CRM boost rectifier with the presented control circuit is implemented. Parameters of the implemented circuit is shown in Table I. $T_{off\text{-}min}$ is set to be 5us. Figs. 3(a) and 3(b) show the steady state operation of the rectifier with 250V input voltage. Traces indicate gate signal, switch current sensed by 0.25Ω resistor, comparator output (v_2 in Fig. 2), and drain-source voltage (v_{ds} in Fig. 2) of the switch from the top. When load current is 0.5A as in Fig. 3(a), the first valley of v_{ds} is detected and causes interrupt to initiate the next switching cycle. If the load is 0.25A as in Fig. 3(b), on the other hand, the first valley is masked because it occurred before the masking time interval. Instead, the second valley is detected and initiates the next switching period. Fig. 3(c) displays the rectifier operation when 220VAC/60Hz line voltage and 100% load are applied. The top two traces indicate line voltage and sensed inductor current, and the bottom one indicates v_{ds}. The rectifier operation is proved to be stable with the 5-us $T_{off\text{-}min}$ throughout the line cycles. If $T_{off\text{-}min}$ is set to zero, the controller cannot update the duty cycle properly and lose the control consequently. In the operation shown in Fig. 3(c), the measured power factor and efficiency are 0.8 and 96.8%. It should be noted that the power factor is measured without any input filter.

4. Conclusion

A digital control implementation for CRM PFC rectifier has been presented in this paper. The control circuit should limit the maximum switching frequency of the rectifier to avoid sever switching loss and lack of calculation time and it is realized by masking the zero current detection which occurred earlier than minimum off-time of main switch. The proposed implementation has been proved to acquire stable operation and high efficiency by 200-W prototype boost rectifier.

Acknowledgment

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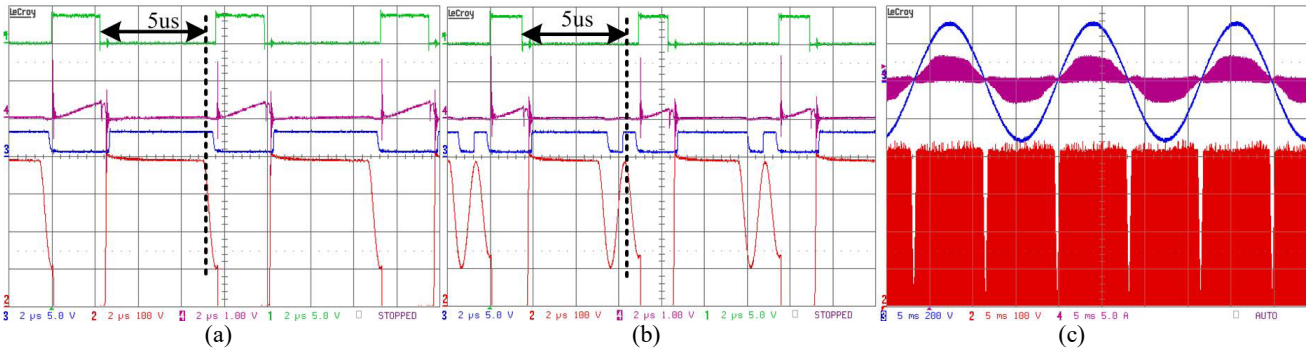

Fig. 3. Experimental waveforms. (a) v_{in} is 250V and load is 0.5A (2us/div). (b) v_{in} is 250V and load is 0.25A (2us/div). (c) v_{in} is 220VAC and load is 0.5A (5ms/div).