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Novel Graphene Volatile Memory Using Hysteresis Controlled by Gate Bias

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Graphene is a carbon based material and it has great potential of being utilized in various fields such as electronics, optics, and mechanics. In order to develop graphene-based logic systems, graphene field-effect transistor (GFET) has been extensively explored. GFET requires supporting devices, such as volatile memory, to function in an embedded logic system. As far as we understand, graphene has not been studied for volatile memory application, although several graphene non-volatile memories (GNVMs) have been reported. However, we think that these GNVM are unable to serve the logic system properly due to the very slow program/read speed. In this study, a GVM based on the GFET structure and using an engineered graphene channel is proposed. By manipulating the deposition condition, charge traps are introduced to graphene channel, which store charges temporarily, so as to enable volatile data storage for GFET. The proposed GVM shows satisfying performance in fast program/erase (P/E) and read speed. Moreover, this GVM has good compatibility with GFET in device fabrication process. This GVM can be designed to be dynamic random access memory (DRAM) in serving the logic systems application. We demonstrated GVM with the structure of FET. By manipulating the graphene synthesis process, we could engineer the charge trap density of graphene layer. In the range that our measurement system can support, we achieved a high performance of GVM in refresh ($>10\ \mu s$) and retention time (~ 100 s). Because of high speed, when compared with other graphene based memory devices, GVM proposed in this study can be a strong contender for future electrical system applications.

Keywords: Graphene, memory, hysteresis