Double-Gate MOSFET Filled with Dielectric to Reduce Sub-threshold Leakage Current

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ABSTRACT

In this work, a special technique called dielectric filling was carried out in order to reduce sub-threshold leakage current inside double-gated n-channel MOSFET. This calibration was done by using SILVACO Atlas(TCAD), and the result showed quite a good performance compared to the conventional double-gate MOSFET.

Index Terms

Double-Gate, Sub-threshold Swing, Silicon-on-Insulator, FinFet, Junctionless FET

Ⅰ. Introduction

As CMOS devices are getting smaller every year due to a lot of smart approaches resolving scalability problems, a brand-new technique filling a dielectric material inside a double-gate NMOS was used in this paper. The double-gate FET was proposed in the early 1980s in thinking of better controlling the short channel effect[1]. This idea has been gradually studied experimentally and theoretically by many different groups[2-5]. Using an insulator inside a planar MOS has been also tried out in the name of SOI(Silicon-on-Insulator) FET for the same reason mentioned above[6]. These two techniques are combined together to obtain a better performance. The reason for setting an insulator in the middle of the double-gate MOS is shown in Figure 1, most leakage current flowing right in the middle.

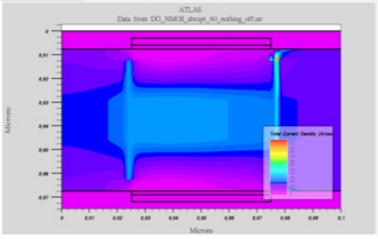

Fig 1. Leakage concentration of a typical Double-Gate MOSFET

Ⅱ. Experiment(Simulation)

Device parameters are as follows: gate length L_g=50nm; gate oxide thickness t_{ox}=1.5nm; silicon body thickness t_{si}=60nm; source and drain doping concentrations $N_S = N_D = 1\times10^{20}cm^{-3}$, n-type; channel doping concentrations $N_{sub} = 1\times10^{18}cm^{-3}$, p-type; drain bias $V_D = 1\,V$; bottom gate voltage $V_{bottom} = 3\,V$ (swept simultaneously with top gate voltage from -3V to 3V), work function of Φ=4.7eV, leakage-blocking oxide thickness $t_{lbox} = 50nm$. Instead of using oxide, simulation when setting air was also tried for the leakage-blocking area. Following figures are structures, energy band diagram(EBD) at off-stage and on-stage, and IV-characteristic of those devices(Fig 1,2,3,4) of an oxide-treated, air-treated, and treated-nothing MOSFETs respectively.

As expected, air-used MOS seems to have a very little leakage current and the least Sub-threshold Swing of 0.0703mV/dec when it is off. However, making the middle of the substrate of MOS empty is almost impossible for fabrication, hence; oxide can be a great alternative which resulted a very much reduced leakage current similar to that of the air-setting

MOS if not better.

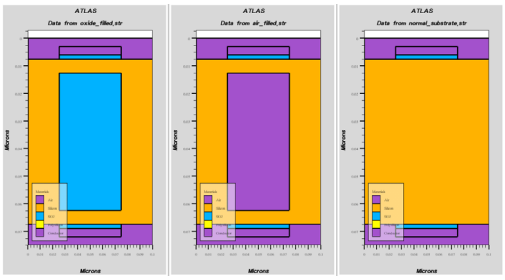

Fig 2. Structure of NMOS treated with oxide, air, and nothing(Si) respectively

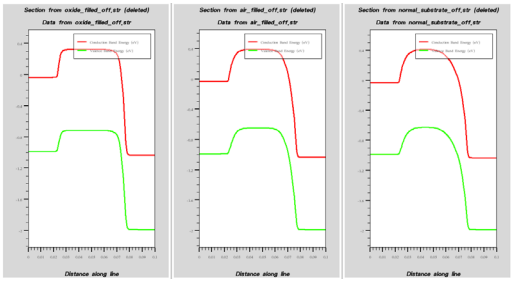

Fig 3. EBD of NMOS treated with oxide, air, and nothing(Si) respectively at off-stage

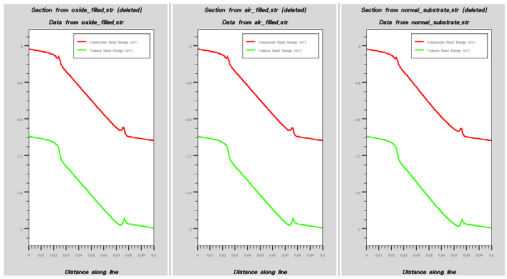

Fig 4. EBD of NMOS treated with oxide, air, and nothing(Si) respectively at on-stage

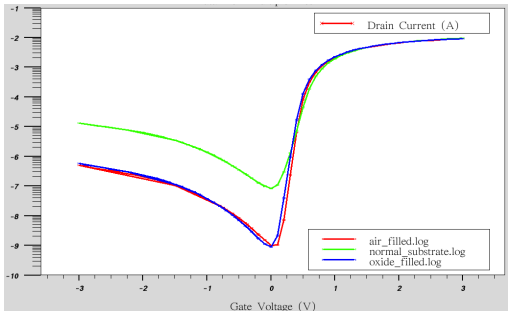

Fig 5. $I_D - V_G$ -characteristic of MOS:
O2: Vt=-1.103V, SS=0.074mV/dec,
Air: Vt=-1.103V, SS=0.0703mV/dec,
Silicon-filled: Vt=-1.103V, SS=0.128 mV/dec

Ⅲ. CONCLUSION

While the DG-SOI-NMOS has shown a nice performance, still, fabrication of the device would not be easy using today's technology. Assuming that fabrication technology develops in the near future, this DG-SOI-NMOS looks quite promising.

What is more, this technique is also applicable to the latest devices like Junctionless FET or FinFET as well, with the same skill that implants oxide inside their substrates.

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