A Novel Inter−Digital Tunable Capacitor for Low−Operation Voltage Applications

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ABSTRACT

In this paper, a tunable capacitor like an interdigital one is presented for low−voltage applications. In order to reduce operation voltage by enhancing fringing electric fields, two finger−patterned electrodes are vertically separated by employing a multi−layer thin film dielectric of a para−/ferro−/para−electrics without spacing between electrodes. The proposed tunable capacitor was fabricated on a quartz wafer and its characteristics are analyzed in terms of effective capacitance and tunability with a function of applied voltages, compared to the conventional interdigital capacitor (IDC). At 8V and 2 GHz, the proposed tunable capacitor shows the tunability of 18 % that is 10.3 % higher than that of the compared one.

Keyword
Tunable interdigital capacitor, ferroelectrics, paraelectrics

Ⅰ. Introduction

The tunable capacitor is the main building block of the reconfigurable RF circuits and systems. There are two types of tunable capacitors; metal−insulator−metal (MIM) and inter−digital capacitors (IDCs), using tunable dielectric thin films. In the case of the MIM capacitors, their characteristics such as tunability, Q−factor, and operation voltage depend mostly on a thickness and quality of a thin−film dielectric. Because of their relatively low operation voltage and high tunability, MIM tunable varactors have employed in various reconfigurable RF circuits [1 − 3]. Contrarily, IDCs operated by enhancing fringing electric fields (fringing E−fields) have often required high−voltage biasing. In order to improve their main performances such as Q−factor, linearity, and tunability, various techniques [4 − 7] have been investigated. The metallization using composite electrodes for high Q−factor was tried [6]. A stacked MIM capacitor to reduce a voltage swing by arranging a number of capacitors in series was developed for improvement of its linearity [7]. An IDC embedding its electrode fully into the thin−film dielectric was proposed [4, 5] for low−voltage operation by more confining fringing electric fields.

In general, a fringing capacitance which is generated in parasitic has a negligible impact on the tunability [8]. In the case of IDCs using mainly fringing electric fields, high− DC voltage required for operation comes from a wide spacing between electrodes compared to thin dielectric thickness of MIM capacitors. And also, in the previous experiment [9], a different interesting result was reported; the fringing capacitance which is generated by using a finger−type electrode can contribute to the tunability.

In this work, a proposed structure of the MIM tunable capacitor like an IDC with zero electrode spacing is presented for low−voltage operation.

II. Design and Fabrication of the proposed tunable capacitor

The fringing electric field is generated at the edge of the metal strip and its strength is higher than that of the center [10]. In the IDC, because its length which passes through in the dielectric is longer than that of the MIM capacitor, its tunability is low, compared to the MIM. The main design factor to determine the tunability of the IDC is the spacing between electrodes. In order to improve the tunability, the narrow spacing is required, however, that means increasing process cost. For the MIM capacitor, when the fringing electric fields are more confined around the electrodes by using special electrodes that enhance fringing electric fields, its tunability can be improved [9].

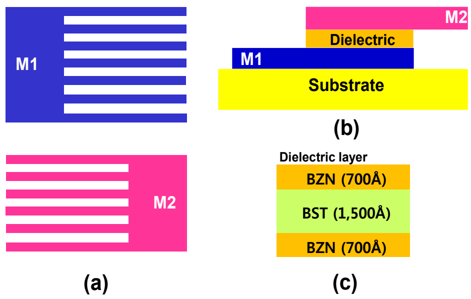

Figure 1. Structure of the proposed novel MIM tunable capacitor: (a) layouts of the electrodes, (b) vertical structure, and (c) structure of the multi-layer thin film dielectrics of BZN/BST/BZN.

Fig.1 shows the structure of the proposed novel MIM tunable capacitor like the IDC. Spacing between electrodes (M1 and M2) is zero. Two electrodes are vertically separated by using the dielectric thin film. The multi-layer dielectric of BZN/BST/BZN is utilized for low-loss and high-tunability purpose. The width of lines and their spacing are 2㎛.

Table 1. Characteristics of the thin-film dielectric.

Dielectric Thin Films	ε_r	tanδ	Tunability
BST (4,000 Å)	250	0.028	48 %
BZN (4,000 Å)	165	0.003	18 %
BZN/BST/BZN (1,000 Å /2,000 Å /1,000 Å)	225	0.005	47 %

Table 1 presents characteristics of each thin-film and multi-layer dielectric used for fabrication of the MIM tunable capacitors for this work. Their characteristics were measured at 10 MHz and 20V by using a metal-insulator-metal (MIM) (Pt/dielectric/Ag) dot (250 µm diameter) capacitor on a Si/SiO_2 (3,000Å)/TiO_2(200Å)/Pt wafer. The multi-layer (BZN/BST/BZN) thin-film dielectric shows a low-loss and high-tunability feature, compared to the lossy BST and low tunable BZN thin-film, respectively.

The tunable capacitors were fabricated on a quartz substrate in coplanar waveguide (CPW) configuration. The first metal (Ti/Pt=100/1,000Å) was deposited and defined as a bottom electrode of the MIM capacitor by using lift-off process. For the multi-layer thin-film dielectric, the first BZN pyrochlore thin-film of 700Å was deposited by RF-magnetron sputtering. The deposition was carried out from stoichiometric $Bi_2(Zn_{1/3}Nb_{2/3})_2O_7$ ceramic target in a high purity O_2/Ar mixture atmosphere. Using the Inductive Coupled Plasma (ICP) dry etcher the BZN film was patterned and then the second thin-film(BST) of 1,500Å was deposited using a B6S4T target and then etched. The final thin-film BZN dielectric of 700Å was deposited and patterned. The photo-lithography and etching process were carried out by using the same photo-mask and dry etcher, respectively, for the multi-layer dielectric. After patterning of each layer, post-annealing processes were carried out at 550℃ for 5 minutes in air to crystallize the film. The lift-off pattern as the second metal (Cr/Au=100Å/1,000Å) was defined on the top of the multi-layer dielectric as the top electrode.

III. Measured Results

The effective capacitance (C_{eff}) and percentage tunability (T) of the fabricated tunable capacitors were analyzed by measuring complex reflection coefficients (S11) with a vector network analyzer (HP8510C) on a probe station.

Fig. 2 (a) shows measured S11 data on the Smith Chart of the fabricated MIM tunable capacitor with the finger-type electrode on the dielectric. The test frequency and DC bias voltage are from 100 MHz to 3 GHz and 0V, respectively. Its self-resonant frequency (SRF) is over 3 GHz. The S11 trace reveals a poor Q-factor that result from thin-thickness of the metal layer. Its analyzed Ceff and tunability as a function of applied DC bias voltage at 2 GHz are shown in Fig. 2 (b). At 25V and 2GHz, its maximum tunability is 38 %.

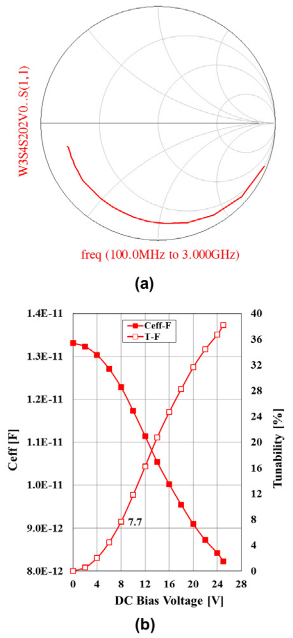

Fig. 2 Measured S_{11} characteristics on the Smith chart (a) and effective capacitance (C_{eff}) and tunability (T) (b) of the tunable capacitor with the finger-type electrode on the dielectric.

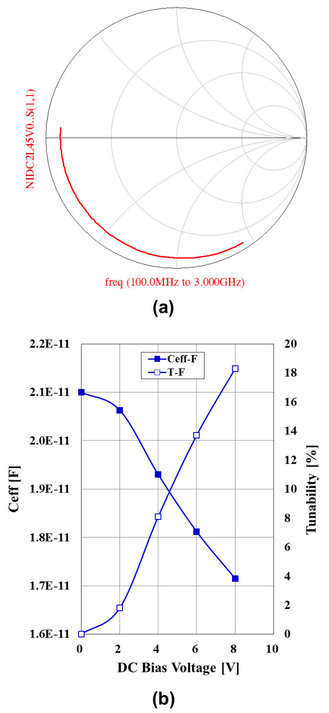

Fig. 3 Measured S_{11} characteristics (a) and C_{eff} and T (b) of the proposed tunable capacitor.

In the Fig. 3, the measured characteristics of the proposed tunable capacitor are shown. Its SRF is over 3 GHz. At 2 GHz, its C_{eff} and T are analyzed as shown in Fig.3(b). Although the overlapped area between two electrodes is much smaller than that of the capacitor in Fig.3, the C_{eff} is higher because of more enhanced fringing electric fields. Also, a break down voltage is low under 10V because the high-intensity electric fields at the edge of the two finger-type electrodes (M1 and M2) are generated. At 8V, the T of the novel architecture is 18% which is an increased value of 10.3%, compared to the capacitor in Fig.3. These results lead to the interesting conclusion that fringing electric fields due to two finger-type electrodes are more generated and they can easily tune characteristics of the thin-film dielectric. However, breakdown voltage is reduced due to their high intensity.

IV. Conclusion

In this paper, an architecture of the tunable capacitor is proposed for low-voltage applications. In order to reduce operation voltage by enhancing fringing electric fields, two finger-patterned electrodes with zero spacing are vertically separated by employing a multi-layer thin film dielectric of a para-/ferro-/para-electrics. The proposed tunable capacitor was fabricated on a quartz wafer and its characteristics are analyzed in terms of effective capacitance and tunability with a function of applied voltages, compared to the tunable capacitor with the finger-pattern electrode only on the top of the dielectric. At 8V and 2 GHz, the proposed tunable capacitor shows the tunability of 18 % that is 10.3 % higher than that of the compared one.

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