Interface engineering for high-k dielectric integration on III-V MOSFETs

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초 록
In this work, we report the comprehensive study of performance enhancement of InGaAs n-MOSFET by plasma PH_3 p assivation. The calibrated plasma PH_3 passivation of the InGaA ssurface before CVD high-k dielectric deposition significantly improves interface quality, resulting in suppressed frequency dispersion in C-V, increase in drive-current with high electron mobility, and excellent thermal stability.

1. 서론

The dominance of silicon technology enabled by geometrical scaling is considered to encounter its downsizing limit in next few generations [1]. Among several emerging technologies and approaches replacing conventional silicon-based planar CMOS devices, III‐V compound semiconductor MOSFETs stand out to hold promise as potential device candidates to be integrated onto the silicon platform for enhancing circuit functionality and also for extending Moore's Law [2]. The development of surface passivation techniques with proper high-k gate dielectric is one of the most critical requirements for successful implementation of III-V MOSFETs. I this work, we report the plasma PH3 passivation on InGaAs channel with HfO2 and HfAlO dielectrics and the performances of n-MOSFETs fabricated by self-aligned gate ‐first process.

2. 본론

By using UHV multi-chamber CVD system, a plasma-PH_3 treatment ($1\%PH_3/N_2$), MOCVD HfO2 ($Hf(OC(CH_3)_3)_4 and O_2$) and HfAlO($HfAl(MMP)_2(OiPr)_5$) deposition, and post deposition annealing were subsequently conducted without breaking vacuum. A sputtered TaN was deposited as gate electrode and patterned by Cl gas based reactive ion etching. S/D was implanted with Si at 50KeV with a dose of $1\times10^{14}cm^{-2}$ and activated at 600ºC for 60 sec, 700ºC 10 sec and 750 ºC 5 sec by RTA (Rapid Thermal Annealing). AuGe/Ni/Au and Ti/Pt/Au contacts were deposited for front and backside contacts.

Fig. 1 shows the I_d-V_g characteristics for the directly deposited and passivated InGaAs n-MOSFET of 4 mm gate length. By using plasma PH_3 passivation, the mean subthreshold slope is 100 mV/dec, I_{on}/I_{off} ratio from 5 orders to 6 orders, drain induced barrier lowering (DIBL) from 92 to 18m V/V.
By grounding the substrate and measuring the capacitance between gate and S/D, the C-V characteristic is measured from low frequency of 500 Hz to high frequency 1 MHz, exhibiting very low frequency dispersion (< 5%).

Thermal stability study of plasma-PH_3 passivated HfAlO/ $In_{0.53}Ga_{0.47}As$gate stack up to 800°C anneal shows the negligible changes in the EOT, frequency dispersion, hysteresis and D_{it}after800°C anneal with slight increase in leakage current and C-V shift (Fig. 2).

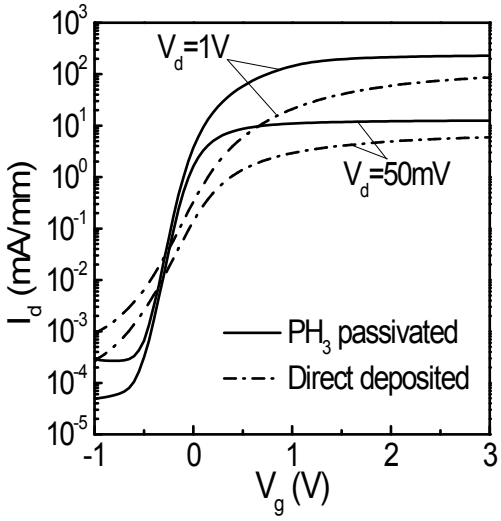

Fig. 1. Drain current at the subthreshold region. I_d-V_g of InGaAs n-MOSFET of 4μm gate length for passivated MOSFET (solid) and directly deposited control (dashed).

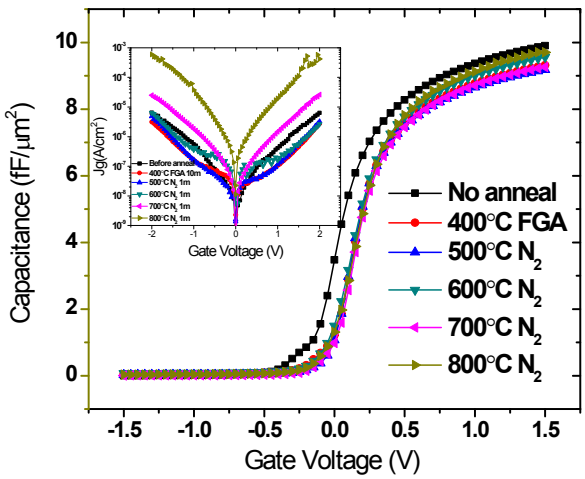

Fig. 2. Split C-V and I-V (inset) curves of Plasma-PH_3 passivated devices measured up to 800°C

3. 결론

In summary, a calibrated plasma PH_3treatment forming a P_xN_y interface layer provides high interface quality and performance improvement for high-k/InGaAs integration.

참고문헌

1.] ITRS 2009 edition
2. S. Takagi et al., VLSI Symposium 147, 2010