EST-008

Surface Preparation of III-V Semiconductors

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As the feature size of Si-based semiconductor shrinks to nanometer scale, we are facing to the problems such as short channel effect and leakage current. One of the solutions to cope with those issues is to bring III-V compound semiconductors to the semiconductor structures, because III-V compound semiconductors have much higher carrier mobility than Si. However, introduction of III-V semiconductors to the current Si-based manufacturing process requires great challenge in the development of process integration, since they exhibit totally different physical and chemical properties from Si. For example, epitaxial growth, surface preparation and wet etching of III-V semiconductors have to be optimized for production. In addition, oxidation mechanisms of III-V semiconductors should be elucidated and re-growth of native oxide should be controlled. In this study, surface preparation methods of various III-V compound semiconductors such as GaAs, InAs, and GaSb are introduced in terms of i) how their surfaces are modified after different chemical treatments, ii) how they will be re-oxidized after chemical treatments, and iii) is there any effect of surface orientation on the surface preparation and re-growth of oxide. Surface termination and behaviors on those semiconductors were observed by MIR-FTIR, XPS, ellipsometer, and contact angle measurements. In addition, photoresist stripping process on III-V semiconductor is also studied, because there is a chance that a conventional photoresist stripping process can attack III-V semiconductor surfaces. Based on the Hansen theory various organic solvents such as 1-methyl-2-pyrrolydone, dimethyl sulfoxide, benzyl alcohol, and propylene carbonate, were selected to remove photoresists with and without ion implantation. Although SPM and DIO3 caused etching and/or surface roughening of III-V semiconductor surface, organic solvents could remove I-line photoresist without attack of III-V semiconductor surface. The behavior of photoresist removal depends on the solvent temperature and ion implantation dose.

Keywords: III-V semiconductor, surface, etching, oxidation

EST-009

Fabrication of a Cu2ZnSn(S,Se)4 thin film solar cell with 9.24% efficiency from a sputtered metallic precursor by using S and Se pellets

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Cu2ZnSn(S,Se)4 thin film solar cells have been fabricated using sputtered Cu/Sn/Zn metallic precursors on Mo coated sodalime glass substrate without using a toxic H2Se and H2S atmosphere. Cu/Sn/Zn metallic precursors with various thicknesses were prepared using DC magnetron sputtering process at room temperature. As-deposited metallic precursors were sulfo-selenized inside a graphite box containing S and Se pellets using rapid thermal processing furnace at various sulfur to selenium (S/Se) compositional ratio. Thin film solar cells were fabricated after sulfo-selenization process using a 65 nm CdS buffer, a 40 nm intrinsic ZnO, a 400 nm Al doped ZnO, and Al/Ni top metal contact. Effects of sulfur to selenium (S/Se) compositional ratio on the microstructure, crystallinity, electrical properties, and cell efficiencies have been studied using X-ray diffraction, Raman spectroscopy, field emission scanning electron microscope, I-V measurement system, solar simulator, quantum efficiency measurement system, and time resolved photoluminescence spectrometer. Our fabricated Cu2ZnSn(S,Se)4 thin film solar cell shows the best conversion efficiency of 9.24 % (Voc : 454.6 mV, Jsc : 32.14 mA/cm2, FF : 63.29 %, and active area : 0.433 cm2), which is the highest efficiency among Cu2ZnSn(S,Se)4 thin film solar cells prepared using sputter deposited metallic precursors and without using a toxic H2Se gas. Details about other experimental results will be discussed during the presentation.

Keywords: CZTS, Thin Fils Solar Cell