Flyback switching loss analysis by capacitor charge and energy conservation

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Abstract

The task of measuring losses becomes more challenging with ever increasing efficiencies and operating frequencies in power electronics applications.[1] Generally, the process of traditional switching loss calculation in flyback converter is very complicated. MOSFET drain-source voltage and current waveforms are needed to calculate switching loss.[2] However, as we know in switched capacitor converter, switching loss can be easily calculated by charge and energy conservation law with known initial and final capacitor voltages.[3] In this paper, the same method is applied to fly-back converter switching loss analysis to simplify calculation procedure.

1. Switching loss modeling

In flyback topology, switching loss is comprised of gate driving loss and MOSFET drain-source voltage-current cross sectional loss. In the first loss term, the gate driver charges and discharges C_{ISS} of MOSFET to turn on and off, which means it could be assumed as C_{ISS} loss term. At the same time, the MOSFET drain-source voltage-current cross sectional loss happens when MOSFET C_{OSS} is charged to a certain level and finally discharged to 0 during switching actions. In other words, total switching loss could be modeled as sum of C_{ISS} loss and C_{OSS} loss in flyback topology.

2. Switching loss analysis

2.1 C_{ISS} loss analysis

Fig.1 shows the schematic of gate driver modeling in C_{ISS} point of view. V_{GATE} is gate driving source with infinite capacitance, I_{GATE} is current that charges C_{ISS} of MOSFET and V_{ISS} is MOSFET C_{ISS} voltage. R_{GATE} is gate driving resistor and L is parasitic inductor between V_{GATE} and V_{ISS}.

Assume that charge stored in C_{GD} is dissipated only by R_{DS_ON} before switch fully turns on (in other words, I_{GATE} only charges C_{ISS} from *0* to V_{GATE} other than dissipating C_{GD}). T and f are switching period and frequency, respectively.

Gate driving current I_{GATE} causes loss in the forms of:

i. Store energy in L (in the form of $\frac{1}{2}L \cdot I_{GATE\_PEAK}^2$).
However, since $I_{GATE} = 0$ at last, energy is also *0*.

ii. Dissipate power in R_{GATE} (in the form of $I_{GATE\_RMS}^2 \cdot R_{GATE}$).

iii. Charge C_{ISS} from *0* to V_{GATE}.

iv. R_{GATE}, L and C_{ISS} energy is lost anyway when gate turns off.

Consequently, total power loss P_{LOSS_CISS} is equal to input charging power P_{GATE} ($V_{GATE} \cdot I_{GATE}$).

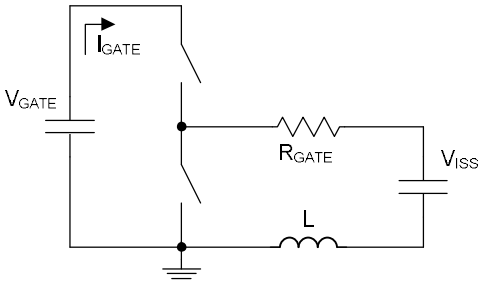

Fig. 1 C_{ISS} loss modeling

According to charge conservation law, I_{GATE} current charges C_{ISS} from *0* to V_{GATE}, which is

$$\int_0^T I_{GATE}(t) \cdot dt = C_{ISS} \cdot V_{GATE} \tag{1}$$

As a result, total C_{ISS} loss is

$$P_{LOSS\_CISS} = P_{GATE} = \frac{V_{GATE} \cdot \int_0^T I_{GATE}(t) \cdot dt}{T} = \frac{V_{GATE} \cdot C_{ISS} \cdot V_{GATE}}{T} = C_{ISS} \cdot V_{GATE}^2 \cdot f \tag{2}$$

2.2 C_{OSS} loss analysis

Fig.2 shows the schematic of MOSFET turn off phase modeling in C_{OSS} point of view. V_{IN} is power source with infinite capacitance, I_{IN} is current that charges C_{OSS} of MOSFET. L_{lk}, L_M and L_P are transformer leakage inductance, magnetizing inductance and primary inductance, respectively. V_{OSS} is MOSFET C_{OSS} voltage, R is primary side parasitic resistor (including PCB pattern and transformer wire resistance).

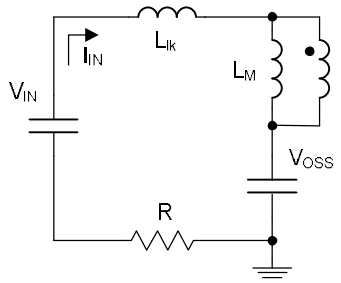

Fig. 2 Schematic of MOSFET turn off phase

Assume that charge stored in C_{GD} is dissipated only by gate driver before switch fully turns off (in other words, I_{IN} only charges C_{OSS} from *0* to a certain level other than dissipating C_{GD}).

Suppose there is no damping effect during C_{OSS} and L_P resonance period and converter is only switching at first valley point. Also suppose that there is no influence of secondary side diode voltage drop and reverse recovery.

As can be seen in Fig.3, C_{OSS} voltage and I_{IN} current waveforms could be divided by 3 states: secondary side diode conducting (*0 – t1*), secondary side diode blocking (*t1 – t2*) and Coss discharging (*t2 – t3*) states.

C_{OSS} charging current I_{IN} causes loss in the forms below during gate turn off phase with secondary side diode conducting:

i. Store energy in L_{lk} (in the form of $\frac{1}{2}L_{lk}\cdot I_{IN\_PEAK}^2$).
However, since $I_{IN} = 0$ at last, energy is also *0*.

ii. Dissipate power in *R* (in the form of $I_{IN\_RMS}^2\cdot R$).

iii. Charge Coss from *0* to $V_{IN}+nV_O$. (C_{OSS_1}: C_{OSS} value at $V_{OSS} = V_{IN} + nV_O$)

Additionally, initial leakage inductor energy is consumed by damping effect of *R*.

C_{OSS} charging current I_{IN} causes loss in the forms below during gate turn off phase with secondary side diode blocking:

i. Store energy in L_P (in the form of $\frac{1}{2}L_P\cdot I_{IN\_PEAK}^2$).
However, since $I_{IN} = 0$ at last, energy is also *0*.

ii. Dissipate power in *R* (in the form of $I_{IN\_RMS}^2\cdot R$).

iii. Discharge C_{OSS} from $V_{IN}+nV_O$ to $V_{IN}-nV_O$. (C_{OSS_2}: C_{OSS} value at $V_{OSS} = V_{IN} - nV_O$)

iv. *R*, *L* and C_{OSS} energy is lost anyway when gate turns on.

Consequently, total power loss P_{LOSS_COSS} is equal to sum of input charging power P_{IN} ($V_{IN}\cdot I_{IN}$) of 2 phases and leakage inductor power loss.

According to charge conservation law, I_{IN} current charges Coss from *0* to $V_{IN}+nV_O$ during *0* to *t1*

$$\int_0^{t1} I_{IN}(t)\cdot dt = C_{OSS\_1}\cdot(V_{IN}+nV_O) \tag{3}$$

As a result, input power from *0* to *t1* is

$$P_{IN\_1} = \frac{V_{IN}\cdot\int_0^{t1} I_{IN}(t)\cdot dt}{T} = \frac{V_{IN}\cdot C_{OSS\_1}\cdot(V_{IN}+nV_O)}{T} = C_{OSS\_1}\cdot V_{IN}\cdot(V_{IN}+nV_O)\cdot f \tag{4}$$

According to charge conservation law, I_{IN} current discharges C_{OSS} from $V_{IN}+nV_O$ to $V_{IN}-nV_O$ during *t1* to *t2*

$$\int_{t1}^{t2} I_{IN}(t)\cdot dt = C_{OSS\_2}\cdot(V_{IN}-nV_O) - C_{OSS\_1}\cdot(V_{IN}+nV_O) \tag{5}$$

As a result, input power from *t1* to *t2* is

$$P_{IN\_2} = \frac{V_{IN}\cdot\int_{t1}^{t2} I_{IN}(t)\cdot dt}{T} = \frac{V_{IN}\cdot(C_{OSS\_2}\cdot(V_{IN}-nV_O) - C_{OSS\_1}\cdot(V_{IN}+nV_O))}{T} = (V_{IN}^2\cdot(C_{OSS\_2}-C_{OSS\_1}) - nV_O\cdot V_{IN}(C_{OSS\_1}+C_{OSS\_2}))\cdot f \tag{6}$$

Total power loss caused by C_{OSS} is

$$P_{LOSS\_COSS} = P_{IN\_1} + P_{IN\_2} + P_{LK} \tag{7}$$

P_{LK} is power stored in leakage inductance and consumed by damping effect,

$$P_{LK} = \frac{1}{2}L_{lk}\cdot I_{IN\_PEAK}^2 \tag{8}$$

2.3 Total loss

Total switching loss is

$$P_{LOSS\_TOTAL} = P_{LOSS\_CISS} + P_{LOSS\_COSS} \tag{9}$$

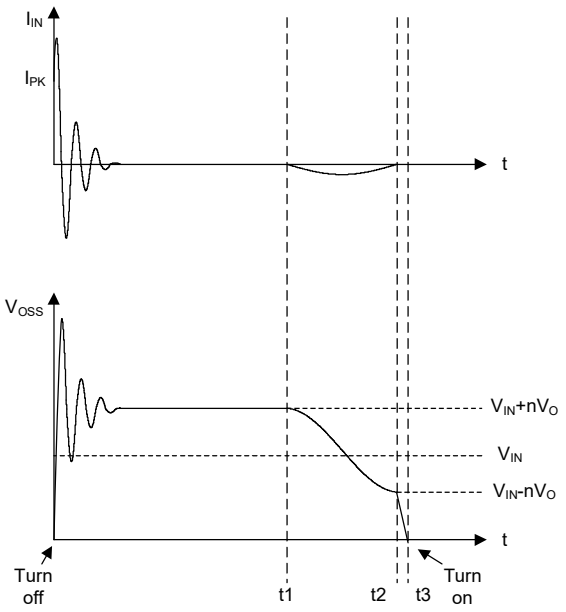

Fig. 3 Equivalent circuit of integrated transformer

3. Summary

This paper proposed a simple method of calculating fly-back converter switching loss only by capacitor charge and energy conservation. Both C_{ISS} loss and C_{OSS} loss are modeled as capacitor loss in combination of voltage source, capacitor, resistor and inductor. All we have to know for switching loss calculation are initial and final capacitor voltages with capacitances at those voltage values. The final calculated value may have some error due to assumptions made to simplify calculation procedure.

References

[1] C. Xiao, G. Chen, and W. G. Odendall, "Overview of Power Loss Measurement Techniques in Power Electronics Systems," Proc. 37th IAS Annual Meeting , pp 1352-1359, October 2002.

[2] Shen, Z.J., Yali Xiong, Xu Cheng, Yue Fu and Kumar, P., "Power MOSFET Switching Loss Analysis: A New Insight" Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE, Vol 3, pp 1438-1442, October 2006.

[3] Ioinovici, A., "Switched-capacitor power electronics circuits", Circuits and Systems Magazine, IEEE, Vol. 1, Issue: 3, pp. 37-42, 2001.