# Compact Model of Tunnel Field-Effect-Transistors

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## Abstract

A compact model of tunnel field effect transistor (TFET) has been developed. The model includes a surface potentia calculation module and a band-to-band-tunneling current module. Model comparison with TCAD shows that the mode calculates TFET surface potential and drain current accurately.

**Index Terms**: drain current, Kane model, surface potential, TFET.

## I. INTRODUCTION

Tunneling field-effect-transistors (TFETS) are considered to be a potential alternative to scaling limits by current CMOS technology. In this regard, development of TFET compact model framework is crucial. A few TFET models have been reported [1]-[3], but their application and choice of tunneling parameters in the band-to-band-tunneling (BTBT) current equation is not clear. The model presents a clear approach to calculate drain current.

## II. TFET MODEL FORMULATION

Fig. 1(a) shows the schematic of an n-type double gate (DG) TFET. Fig. 1(b) shows its band diagram in off and on states. Tunneling takes place at the source-channel junction. The gate field controls the BTBT process by pushing down or up the channel conduction band until it becomes lower or higher than source valence band, thereby turning the device on or off, respectively.

The model divides DG-TFET in three regions. Region I includes the source region, region II includes the source-body tunneling region, and region III includes the channel region. Based on its operation principles, region I and II are equivalent to a gated-tunnel diode, and region III is equivalent to a DG-MOSFET channel region. 2-dimensional Poisson equations are solved to obtain surface potential across regions I and II. Surface potential in region III is obtained using Lambert function based explicit analytical surface potential model for DG-MOSFET [4].

After matching the boundary conditions [1], including surface potential and electric field at the junction of region I and II, surface potential at x=0, lengths of region I and II, and the surface potential profile along channel length can be found and are listed below, respectively [1].

$$\varphi_s(0) = -\sqrt{[V_{gs} - V_{fbs} - (V_{bis} + \varphi_{dg})]^2 + 2(V_{gs} - V_{fbs})\emptyset + \emptyset^2}$$
$$+(V_{gs} - V_{fbs} + \emptyset), \emptyset = \frac{qN_{seff}\lambda_{II}^2}{\varepsilon_{si}} \quad (1)$$

$$L_1 = \sqrt{\frac{2\varepsilon_{si}\varphi_s(0)}{qN_{seff}}} \quad (2)$$

$$L_2 = \lambda_{II}\cosh^{-1}\left[-\frac{\varphi_s(0)-(V_{gs}-V_{fbs})}{(V_{gs}-V_{fbs})-(V_{bis}+\varphi_{dg})}\right]. \quad (3)$$

$$\varphi_{s1} = \frac{qN_{seff}}{2\varepsilon_{si}}(x + L_1)^2 \quad (4)$$

$$\varphi_{s2} = (V_{gs} - V_{fbs}) - [V_{gs} - V_{fbs} - V_{bis} - \varphi_{dg}].\cosh(\frac{x-L_2}{\lambda_{II}}). \quad (5)$$

Minimum tunneling length can be found using equations (4) and (5) and is expressed as,

$$W_t = L_1 + L_2 - \lambda_{II}.\cosh^{-1}\left(\frac{V_{gs}-V_{fbs}-\varphi_I}{(V_{gs}-V_{fbs})-(V_{bis}+\varphi_{dg})}\right) - \sqrt{\frac{2\varepsilon_{si}}{qN_{seff}}(\varphi_I) - \frac{E_g}{q}} \quad (6)$$

Average electric field is computed by,

$$E_{avg} = \frac{E_g}{qW_t}. \quad (7)$$

Finally, drain current expression is given by [5],

$$I_{ds} = qt_{si}A_kW_tE_{avg}{}^2\exp\left(-\frac{B_k}{E_{avg}}\right). \quad (8)$$

## III. DISCUSSION AND CONCLUSION

The model was compared with TCAD simulation [6] to prove the validity of the model. Device parameters for the simulated device were $t_{ox}$=1 nm, $t_{si}$=10 nm, $L_{ch}$=50 nm, $N_s$=$N_d$=$10^{20}$ /cm$^3$, $N_{ch}$=$10^{12}$ /cm$^3$.

Fig. 2 shows surface potential profile along channel length for different $V_{gs}$ values. Both the model and simulation are in good agreement. Fig. 3 shows $I_{ds}$-$V_{gs}$ for different $V_{ds}$ values. Both simulation and model are in good agreement. Fig. 4 shows $I_{ds}$-$V_{ds}$ for different $V_{gs}$ values. Intercept and slope of log of Eq. (8) was calculated to extract $A_k$ and $B_k$ values, respectively, with $I_{ds}$ from the simulator, and $E_{avg}$ calculated from the model [6]. $A_k$ and $B_k$ values are mentioned in Table 1.

Overall, the model produces excellent results compared to simulation. The approach presented here attempts to clear some confusion in application of reported models.

**Table 1.** $A_k$/$B_k$ values as a function of $V_{ds}$

| $V_{ds}$ | $A_k$ (/V$^2$.s) | $B_k$ (V/cm) |
|---|---|---|
| 0.10 | 1.5x10$^{18}$ | 29.74 M |
| 0.15 | 1x10$^{19}$ | 29.74 M |
| 0.20 | 2x10$^{19}$ | 29.74 M |
| 0.25 | 3x10$^{19}$ | 29.74 M |
| 0.30 | 3x10$^{19}$ | 29.74 M |
| 0.35 | 3.3x10$^{19}$ | 29.74 M |
| 0.40 | 3.5x10$^{19}$ | 29.74 M |
| 0.45 | 3.5x10$^{19}$ | 29.74 M |
| 0.50 | 3.5x1$^{19}$ | 29.74 M |
| 0.55 | 3.8x10$^{19}$ | 29.74 M |
| 0.60 | 3.8x10$^{19}$ | 29.74 M |
| 0.65 | 3.8x10$^{19}$ | 29.74 M |
| 0.70 | 4.0x10$^{19}$ | 29.74 M |
| 0.75 | 4.1x10$^{19}$ | 29.74 M |
| 0.80 | 4.28x10$^{19}$ | 29.74 M |
| 0.85 | 4.37x10$^{19}$ | 29.74 M |
| 0.90 | 4.45x10$^{19}$ | 29.74 M |
| 0.95 | 4.52x10$^{19}$ | 29.74 M |
| 1.0 | 4.60x10$^{19}$ | 29.74 M |

## ACKNOWLEDGMENTS

This research was supported by the MOTIE(Ministry of Trade, Industry & Energy (project number: 10054888) and KSRC(Korea Semiconductor Research Consortium) support program for the development of the future semiconductor device.

## REFERENCES

[1] L. Zhang, J. He and M. Chan, "A compact model for double-gate tunneling field-effect-transistors and its implications on circuit behaviors," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, San Francisco, CA, 2012, pp. 6.8.1-6.8.4.

[2] R. Vishnoi and M. J. Kumar, "Compact Analytical Model of Dual Material Gate Tunneling Field-Effect Transistor Using Interband Tunneling and Channel Transport," *IEEE Transactions on Electron Devices*, Vol. 61, No. 6, pp. 1936-1942, June 2014.

[3] J. U. Mehta, W. A. Borders, H. Liu, R. Pandey, S. Datta and L. Lunardi, "III–V Tunnel FET Model With Closed-Form Analytical Solution," *IEEE Transactions on Electron Devices*, Vol. 63, No. 5, pp. 2163-2168, May 2016.

[4] A. Ortiz-Conde, F. J. Garcia-Sanchez, and S. Malobabic, "Analytic solution of the channel potential in undoped symmetric dual-gate MOSFETs," *IEEE Trans. Electron Devices*, Vol. 52, No. 7, pp. 1669–1672, Jul. 2005.

[5] X. Huifang, D. Yuehua, L. Ning, and X. Jianbin, "A 2-D Semi-Analytic Model of Double-Gate Tunnel-Field Transistor," *Journal of Semiconductor*, Vol. 36, No. 5, 2015.

[6] ] ALTAS Device Simulation Software, Silvaco Int., Santa Clara, CA, USA, Version 5.20.2.R, 2015.

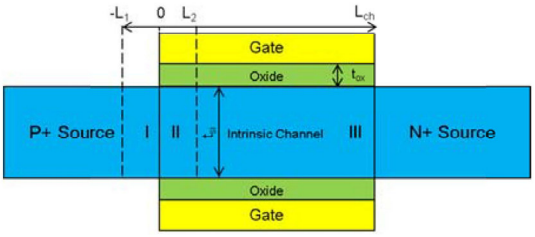


**Fig. 1(a).** Schematic of DG-TFET device.

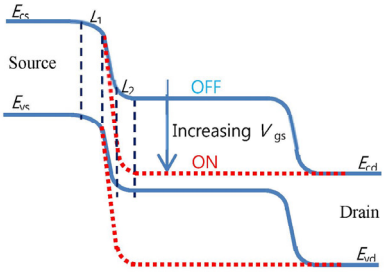


**Fig. 1(b).** Band diagram of TFET device.

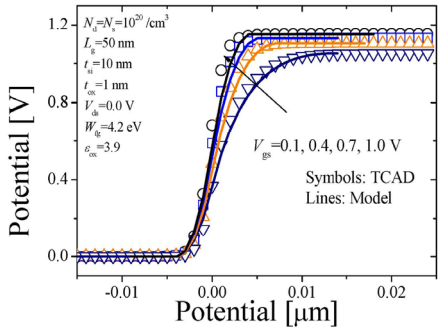


**Fig. 2(a).** Surface potential profile along channel length calculated from model (lines) compared with simulation (symbols) for $V_{ds}$=0.0 V

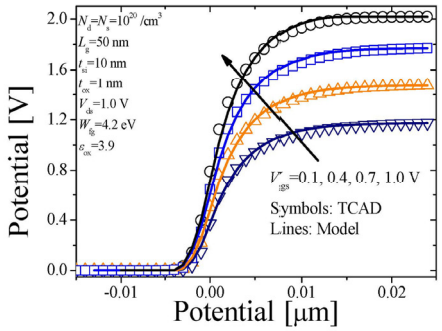


**Fig. 2(b).** Surface potential profile along channel length calculated from model (lines) compared with simulation (symbols) for $V_{ds}$=1.0 V.

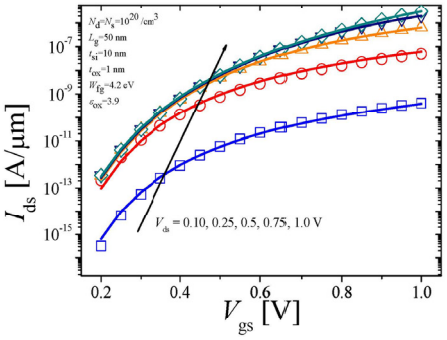


**Fig. 3.** $I_{ds}$-$V_{gs}$ for different $V_{ds}$ values, calculated from the model (lines) compared with simulation (symbol).

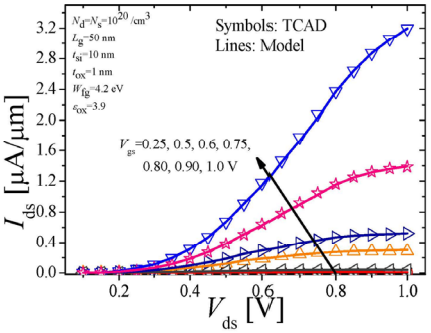


**Fig. 4.** $I_{ds}$-$V_{ds}$ for different $V_{gs}$ values, calculated from the model (lines) compared with simulation (symbol).