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Analysis of a First Order Multilevel Quantized DPLL with Phase-and Frequency-Step Input

(多値 量子化한 一次 DPLL의 位相과 周波數 스텝 入力에 대한 解析)

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要 約

入力信號와 比較信號와의 時間誤差를 多値 量子化하는 時間 誤差 檢出器(TED)를 考察하여 새로운 形態의 디지탈 位相固定回路(DPLL)를 提案하고 性能을 解析하였다. 本 論文에서 考案된 TED는 線形的인 特性을 갖게 되므로 DPLL의 動作은 線形 差分 方程式으로 解析된다. 雜音이 없는 경우에, 誘導된 시스템 方程式을 解析하여 提案된 DPLL 入力信號의 初期 時間誤差에 관계없이 入力信號의 位相과 周波數를 追跡할 수 있는 條件 및 그에 따른 周波數 追跡 範圍를 구했으며 타이밍 에러 플레인(timing error plane) 方法 및 컴퓨터 시뮬레이션을 통해 앞에서 해석된 결과들이 잘 一致함을 보였다.

Abstract

A new type of digital phase-locked loop (DPLL) that employs a multilevel quantized timing error detector (TED) is proposed and analyzed under the assumption of negligible quantizing effect and no noise. Since the timing error is quantized uniformly, the TED has a linear characteristic. From the linear characteristic of TED, a first order difference equation describing the behavior of the loop is derived.

Using the system equation, the loop is analyzed mathematically for phase step and frequency step input. Desired locking condition for the loop to be locked and the lock range for the DPLL's to achieve exact locking independently of initial conditions are obtained. And these analyses are confirmed by timing error plane plots and computer simulation.

I. Introduction

Phase-locked loops have been used in various parts of telecommunication systems because of their wide applicability to bit synchronization and FM- and PM- demodulation, etc.[1] Since the late 1960's, various types of digital phase-locked loops (DPLL's) have been studied due to the increased reliability and decreased cost of integrated digital circuitry.[2~5] DPLL's of the type employing multilevel quantized phase detection and discrete phase adjustment also have been studied for sinusoidal input and rectangular input.[6,7] The behavior of those DPLL's is, however, much restricted and difficult to be analyzed because of their nonlinear phase detector characteristics.

This paper deals with a comprehensive

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and complete analysis of a first order multilevel quantized DPLL that tracks the zero crossings of the incoming signal – assuming negligible quantizing effect and no noise. Unlike other DPLL's, this loop has a unique property in that the timing error (not phase error) which is the time difference between input signal and reference signal controls the digitally controlled oscillator (DCO) directly. Since the timing error detector (TED) has a linear characteristic, the loop is characterized by a linear difference equation in time domain.

The loop is also analyzed easily by using timing error plane plots. In section II basic relationships of the proposed loop are presented and the loop equation describing the loop behavior is derived. In section III analyses of the loop are carried out in the absence of noise. Desired locking condition and lock range are also explained.

II. Mathematical Model of the Loop

This loop is an all digital phase-locked loop made up of three parts: a multilevel quantized TED, a loop filter and a DCO. Fig. 1 shows the

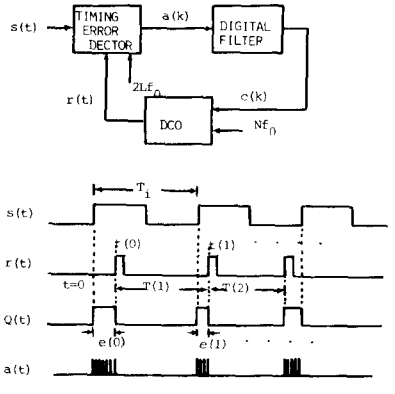


Fig. 1. System blcok diagram and the relation between each signal.

block diagram of the loop and the relation between each signal. The input signal is considered to be a rectangular waveform. The multilevel quantized TED is composed of one Flip-Flop and some logic Gate's. We can get LEAD signal by making s(t) and Q(t) AND-gated. LAG signal is obtained by making $\bar{s}(t)$ and Q(t) AND-gated, where $\bar{s}(t)$ is inverted signal of s(t). Then the TED detects how much the input signal leads or lags the reference signals as shown in Fig. 2. The output of the filter, i.e., the correction signal changes the clock period of DCO in such a way to decrease the timing error.

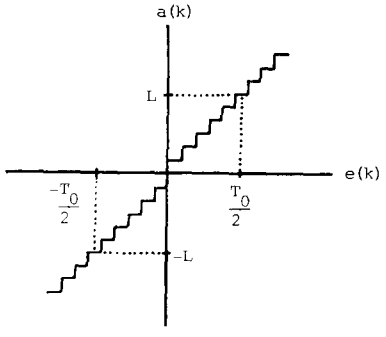


Fig. 2. Characteristic of a multilevel quantized TED.

Let t(k) denote the time elapsed up to k_{th} clock period of the DCO, then it can be expressed as follows.

$$t(k) = t(0) + \sum_{j=1}^{k} T(j) \qquad (1)$$

where t(0) is an initial timing error and T(j) is the time interval between t(j-1) and t(j). Let e(k) denote the timing error between s(t) and r(t), it can be expressed as follows.

$$e(k) = t(k) - kT_i \qquad (2)$$

where T_i is the period of the input signal. And the output of the TED is given by

$$a(k) = \frac{2L}{T_o}\, e(k) \qquad (3)$$

where T_o is the nominal clock period of the DCO and L is the number of quantizing levels for the interval $T_o/2$. The correction signal c(k) is given by

$$c(k) = \frac{T_o}{N} a(k) D(z) \quad (4)$$

For a first order DPLL, the loop filter represents just a proportional constant, i.e., $D(z) = K$. Thus (4) becomes

$$c(k) = \frac{2L}{N} K \; e(k) \quad (5)$$

where N is the number of DCO input clock pulses during the nominal clock period T_o.

The correction signal c(k) is used to control the next period of r(t) according to the following algorithm.

$$T(k) = T_o - c(k-1) \quad (6)$$

From (1) and (6), we have

$$t(k) = t(0) + kT_o - \sum_{j=1}^{k-1} c(j) \quad (7)$$

From (2) and (7), the following difference equation describing the loop behavior is derived.

$$e(k+1) = (1 - \frac{2L}{N} K)\, e(k) + (T_o - T_i) \quad (8)$$

III. Loop Analysis

1. Phase Step Response

For a phase step input, only an initial timing error exists, i.e. $T_i = T_o$. So the system equation (8) reduces to

$$e(k+1) = (1 - \frac{2L}{N} K)\, e(k) \quad (9)$$

In the steady state, if one exists, both e(k+1) and e(k) are equal to e_{ss}, the steady state timing error. Thus, in the steady state $e_{ss} = (1 - \frac{2L}{N} K)\, e_{ss}$.

Accordingly, e_{ss} must be zero as expected. If $\frac{2L}{N} K$ is equal to one, e(k+1) will be identically zero. Hence $\frac{L}{N} K = \frac{1}{2}$ may be considered to be "optimum" in the sense that it yields the rapidest convergence to a steady state. Similar results have been shown in other types of DPLL's.[8,9]

Let z-transform of e(k) be E(z) and taking z-transform of (9), then we have

$$E(z) = \frac{e(0)\, z}{1 - \frac{2L}{N} K} \quad (10)$$

Taking inverse z-transform of (10), e(k) is given by

$$e(k) = (1 - \frac{2L}{N} K)^k e(0) \quad (11)$$

Since e(k) must become zero in the steady state, the condition for the loop to be locked is given by $|1 - \frac{2L}{N} K| < 1$. Accordingly, the desired locking condition is

$$0 < \frac{L}{N} K < 1 \quad (12)$$

The behavior of the loop can be also explained graphically by drawing the timing error plane plots corresponding to the system equation. Fig. 3 shows the timing error plane plots for different values of $\frac{L}{N} K$. In Fig. 3, (a)-(c) represent the case of locking and (d) represents the case of divergence. In these figures, subsequent points can be determined along the arrows from the initial point e(0).

A computer simulated results of locking procedure with phase step input is shown in

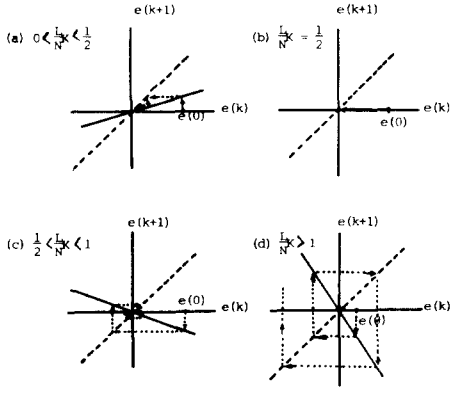


Fig. 3. Timing error plane plots with phase step input.

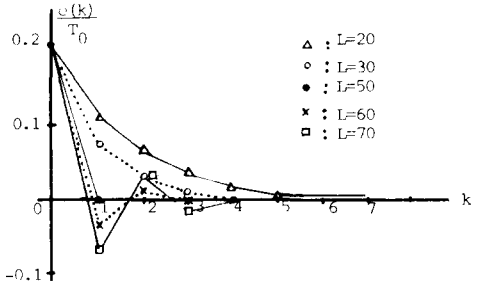


Fig. 4. Locking procedure with an initial timing error.

Fig. 4. The following parameter values are assumed: N =100, K = 1, e(0) = 0.2 T_o. It is shown that L = 50 makes one step locking, while other values of L need several steps to attain a steady state.

2. Frequency Step Response

When the input signal has a frequency offset initially, T_i is not equal to T_o. Under the steady state condition, e(k+1) and e(k) are equal to e_{ss}. Then (8) becomes

$$e_{ss} = (1 - \frac{2L}{N}K)\, e_{ss} + (T_o - T_i) \tag{13}$$

Consequently, we have the steady state timing error given by

$$e_{ss} = \frac{T_o - T_i}{\frac{2L}{N}K} \tag{14}$$

Solving (8) for e(k) by using z-transform, we obtain

$$e(k) = (1-\frac{2L}{N}K)^k \left[e(0) - \frac{N}{2LK}(T_o - T_i)\right] + \frac{N}{2LK}(T_o - T_i) \tag{15}$$

For the loop to be stable, e(k) must converge as k becomes large. From this, we obtain the following condition.

$$|1 - \frac{2L}{N}K| < 1$$

Thus, a desired condition for the loop to be locked with frequency step input is the same as the one with phase step input.

In order to achieve an exact locking, in addition to (12), the following two conditions have to be satisfied.

i) The value of e_{ss} must be always in the interval $(-\frac{T_i}{2}, \frac{T_i}{2})$. From the above condition, we obtain the following inequality.

$$1 - \frac{L}{N}K < \frac{T_o}{T_i} < 1 + \frac{L}{N}K \tag{16}$$

ii) The value of e(k+1) must be in interval $(-\frac{T_i}{2}, \frac{T_i}{2})$, whatever value e(k) may have. This condition is expressed as

$$1 - \frac{L}{N}K < \frac{T_o}{T_i} < 1 + \frac{L}{N}K \quad , \text{if } \frac{L}{N}K \le \frac{1}{2} \tag{17-a}$$

$$\frac{L}{N}K < \frac{T_o}{T_i} < 2 - \frac{L}{N}K \quad , \text{if } \frac{L}{N}K \ge \frac{1}{2} \tag{17-b}$$

Equation (17) contains all the cases of (16). Therefore the lock range is given by

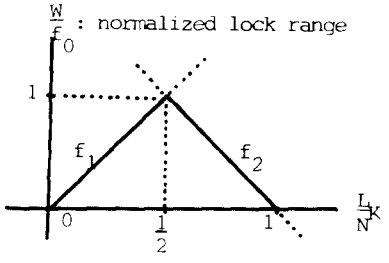
$$1 - \frac{L}{N}K < \frac{f_i}{f_o} < 1 + \frac{L}{N}K \quad , \text{if } \frac{L}{N}K \le \frac{1}{2} \tag{18-a}$$

$$\frac{L}{N}K < \frac{f_i}{f_o} < 1 + \frac{L}{N}K \quad , \text{if } \frac{L}{N}K \ge \frac{1}{2} \tag{18-b}$$

where $f_o = \frac{1}{T_o}$: free running frequency of the DPLL

The lock range for different values of $\frac{L}{K}K$ is obtained from (18) as shown in Fig. 5. It is shown that $\frac{L}{N}K = \frac{1}{2}$ makes the widest lock range. The same result is shown in Fig. 7.

Fig. 6 shows the timing error plane plots with frequency step input. Fig. 6(a) is for $0 < \frac{L}{N}K < \frac{1}{2}$ and represents the case of monotonous locking process. Fig. 6(b) is for $\frac{L}{N}K = \frac{1}{2}$ and represents the case of one step locking. In this case, the loop makes the widest lock range. Fig. 6(c) is for $\frac{1}{2} < \frac{L}{N}K < 1$ and represents the case of oscillatory locking process.



$$f_1 = \frac{2L}{N}K \qquad f_2 = 2 - \frac{2L}{N}K$$

Fig. 5. Lock range for different values of $\frac{L}{N}k$.

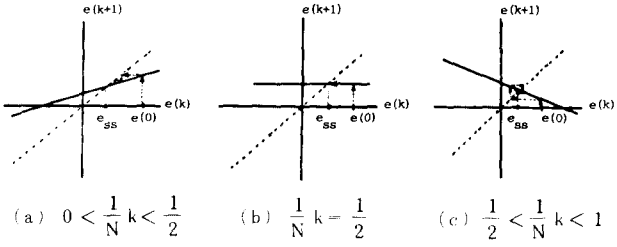


Fig. 6. Timing error plane plots with frequency step input.

The steady state timing error is determined by the crossing point of solid line and the dotted line in Fig. 6.

The relationship between steady state timing error e_{ss} and input frequency f_i, as the parameter of $\frac{L}{N}K$, is shown in Fig. 7. N = 100 and K = 1 are assumed in simulation results.

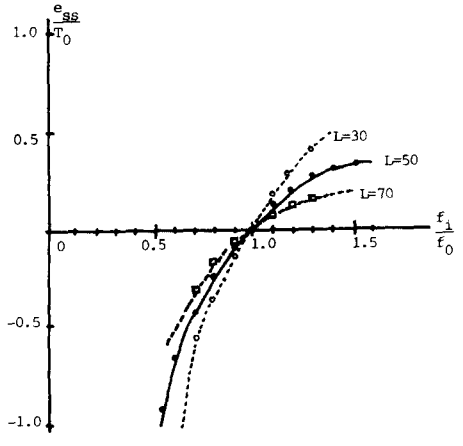


Fig. 7. The relation between e_{ss} and $\frac{L}{N}K$.

VI. Conclusion

In this paper, a new type of DPLL using a multilevel quantized timing error detector is proposed ans analyzed under the assumption of negligible quantizing effect and no noise. Since the devised TED has a linear characteristic, the loop behavior is described by a linear difference equation.

The basic system equation is derived and analyzed with phase- and frequency step input. The desired locking condition and the lock range are obtained in closed forms. And these analyses are confirmed by computer simulation.

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