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Performance of a Digital PN Sequence Acquisition System

(디지탈 PN 초기 동기장치의 성능)

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要 約

본 논문에서는 direct sequence(DS) 방식을 이용한 spread spectrum system에 사용할 수 있는 빠른 초기 동기 방법을 제안하였다. 수식적인 모델을 세우고 해석을 한 후 computer simulation을 거쳐 제안된 system의 성능을 분석하여 sliding correlator에 비해 우수함을 입증하였다. 입력 신호의 signal-to-noise ratio(SNR)가 −18dB에서 초기 동기 시간이 45ms 소요되었다. 이 방법의 hardware 구현과 실험 결과도 설명하였다.

Abstract

A fast pseudo-noise (PN) sequence acquisition algorithm for the direct-sequence (DS) spread spectrum system is proposed. The basic concept of the algorithm has been adopted from that of the classical sliding correlator. Mathematical modeling, analysis and computer simulation of the proposed system have been done. The results of analysis and computer simulation show that the acquisition system yields a significant performance improvement over the sliding correlator. Its acquisition time takes only 45 ms when signal-to-noise ratio (SNR) is -18dB. The algorithm developed has been implemented in hardware and its experimental result is also given.

I. Introduction

One important subsystem in a direct-sequence (DS) spread spectrum system is the pseudo-noise (PN) code acquisition system in which the PN code sequence of the receiver is aligned with the transmitted code within one chip interval.

Since the development of spread spectrum concepts, many different PN sequence acquisition methods have been proposed. The sliding correlator that has been used most widely for PN sequence acquisition is the simplest one among various correlation techniques. Although it is simple, one drawback of the sliding correlator is that the search speed is limited by the response time of the post correlation receiver. Ward proposed acquisition techniques called RASE[1] and RARASE.[2] These methods are advantageous for rapid

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synchronization. He showed that acquisition time can be improved by a factor of more than 100 by using these techniques instead of the sliding correlation method. The techniques, however, have a disadvantage in that they are more vulnerable to interfering signals than other techniques.[3]

In this paper we propose a new digital PN code acquisition system that may be used as a subsystem of the direct sequence (DS) spread spectrum communication system. The basic concept of the system algorithm has been borrowed from that of the classical sliding correlator. The acquisition system presented in this paper can acquire PN sequences rapidly under adverse conditions where SNR is lower than -18 dB.[1] Also, it can be implemented simply in hardware.

Following this introduction, we first describe the algorithm of the proposed acquisition system in section II. In section III we analyze the performance of the system including acquisition time and probability of false lock. In section IV we discuss the method of computer simulation, and compare the simulation result with the analytical result. Also, the performance of the proposed system will be compared with those of other acquisition systems. In section V we describe hardware implementation of the proposed acquisition system. Finally, we make conclusions in section VI.

II. Description of the Acquisition System

A block diagram of the proposed PN sequence acquisition system is shown in Fig. 1. In this system the incoming signal is filtered by a wideband filter to reduce out-of-band noise and interference. Then, the filtered signal is sampled in 1-bit binary sequences by the samplers 1 and 2. These samplers sample the signal at the same rate as the PN code sequence. The sampling is offset by one half-bit interval with respect to each other. Therefore, if we take two estimates from the incoming signal per 1-bit interval, at least one of the two estimates will be sampled at the point from which the center of incoming code bit is never apart more than one half-bit interval.

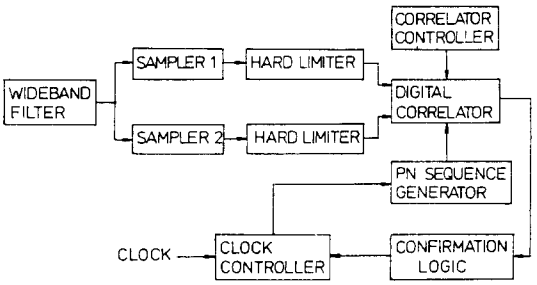

Fig. 1. Block diagram of the proposed PN sequence acquisition system.

The process of PN sequence acquisiton is divided into two; the search process and the verification process. The actual search process of incoming PN code phases is performed by a correlator. In the search stage, the two sequences are correlated with the local PN code sequence at the same time. Then, each correlation result is compared with the threshold of the search stage. If both the correlation results do not exceed the threshold, another set of estimates are fed into the correlators while the local PN code sequence is kept from advancing. This process is, in effect, the same as sliding the incoming signal with respect to the local PN code phase. If one or both of correlation values exceeds the threshold during the search process, the verification process starts. At this time the local PN sequence generator is permitted to generate a PN code sequence. It is reasonable to assume that the sequence from which synchronization is found in the search process has less estimation error than the other se-

[1] We have designed this system with the code rate of 5 M bits/s (Mbps) and the voice transmission rate of 32 Kbps. Thus, this system has 22 dB process gain. Accordingly, the system has the error rate about 10^{-2} at the SNR of -18 dB when coherent phase-shift keying demodulation is used. These values are our design goal at the worst case.

quence. Hence, unlike the search process, in the verification process we use only one sequence that has greater correlation value, and discard the remaining one.

In the verification process as well as the search process, there are two important parameters to be considered. One is false alarm probability[4] denoted by P_{fa}, and the other is false dismissal probability denoted by P_{fd}. The sources of these errors can be divided into two categories. One is the error resulting directly from estimation, and the other is the error originated from side lobes (or minor peaks) of the partial correlation function. Since we select the sequence that has less estimation errors at the end of the search process, we must increase the length of partial correlation to minimize the second category of errors, thereby lowering the false alarm and false dismissal probabilities.

Another point to be considered in determining the partial correlation length in the verification process is the time required for verification of false synchronization point resulting from a false alarm error. During the verification stage the sliding process is stopped, and therefore, acquisiton time is increased by the same amount as used for verification. Hence, in the proposed acquisition system, the length of partial correlation is increased gradually by 64 bits per every step to reject the false alarm with relatively short verification time.

A flow diagram for the operation of verification is shown in Fig. 2. As seen in the figure, once any of the correlation values of the two estimated sequences exceeds the threshold in the search stage, the lock of the local PN sequence generator starts to run, and the correlator accepts the next 128 bits of the estimated incoming signal and the local PN code sequence. When the 128 bits of data are accepted, the comparator compares the correlation value of the accepted 128 bits of data with the threshold. If the correlation value does not exceed the threshold, the local PN code generator stops again, the whole

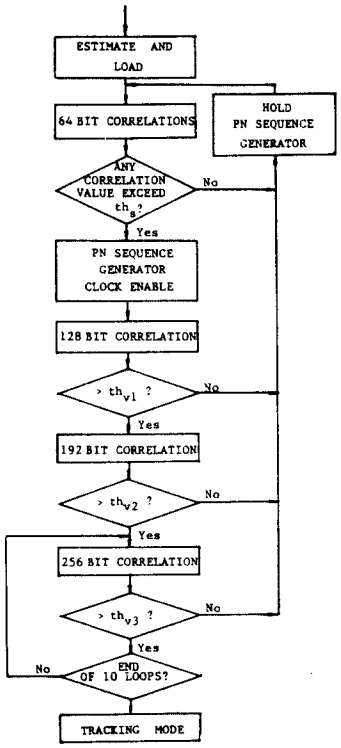

Fig. 2. Flow diagram of the proposed algorithm.

process returns to the starting point for another search process. If the threshold is exceeded, the second verification stage is permitted to start. The second verification stage is the same as above except that the lelngth of partial correlation is 192 bits long. After the second verification stage is passed successfully, the third verification stage starts, in which verification with 256-bit partial correlation is to minimize false lock probability that is an important parameter in evaluating the performance of the PN sequence acquisition system.

III. Performance Analysis

The first step in the PN acquisition process of the proposed system is to convert the incoming signal into 1-bit binary sequences and correlate it with a local PN sequence. Since the digital correlator performs bit-by-bit comparison, and the correlation value is the

same as the number of agreements in comparison, one can represent the correlation results in two types as follows. When the phase of the local PN sequence is the same as that of the incoming signal, the correlation value becomes equal to the number of correlated bits or correlation length, providing that there are no random binary errors occurring as a result of the interference at the input of the estimator. In this case, the probability distribution function of correlation results becomes simply the binomial distribution. Hence, the probability of having i bits of errors in L bit correlation becomes

$$P_{sync}(i) = \binom{L}{i} p^i (1-p)^{L-i} \tag{1}$$

where L is the length of correlation, p denotes the probability of error in the estimator, and $\binom{L}{i} = \frac{L!}{(L-i)!\, i!}$. On the other hand, when the phase of the local PN sequence is not the same as that of the incoming signal, one can approximate the distribution to the binomial distribution under the following conditions. That is, the correlation length L must be large enough compared with the number of stages in the PN sequence generator, and the probability of estimation error, which increases randomness of the PN sequence, must be greater than 0.15 [12]. Under these conditions the results of each bit-by-bit comparison can be regarded as Bernoulli random variables with p=½. Accordingly, we write probability distribution as

$$P_{unsync}(k) = \binom{L}{k} (½)^L \tag{2}$$

where k is the number of agreements in L bit correlation.

Using (1) and (2), we can obtain false alarm and false dismissal probabilities, P_{fa}^L and P_{fd}^L, for L-bit correlation with a given threshold as the following:

$$P_{fa}^L(th) = \sum_{k=th}^{L} P_{unsync}(k) = \sum_{k=th}^{L} \binom{L}{k} (½)^L \tag{3}$$

$$P_{fd}^L(th) = \sum_{i=L-th+1}^{L} P_{sync}(i) = \sum_{i=L-th+1}^{L} \binom{L}{i} p^i (1-p)^{L-i} \tag{4}$$

where 'th' denotes threshold for a given correlation length L. And the correct decision probability can be obtained as

$$P_c^L(th) = 1 - P_{fd}^L(th). \tag{5}$$

For the ease of analysis, let us use a state transition diagram shown in Fig.3. With the aid of the state transition diagram and (3), (4) and (5), we can derive the exact expression of the mean acquisition time. To derive the equation of the mean acquisition time, the cost functions of false alarm and false dismissal are calculated as follows. The physical meaning of the cost functions are as follows. The cost function of false alarm represents the average number of bit time intervals required to slide the phase of the local PN sequence, since the sliding process stops for verification when the false alarm occurs. Likewise, the cost function of false dismissal represents the number of bit time intervals that are used for verification of synchronization which is dismissed during the verification even though the phase of the local PN sequence is correct. The cost function of false alarm in the first verification stage is

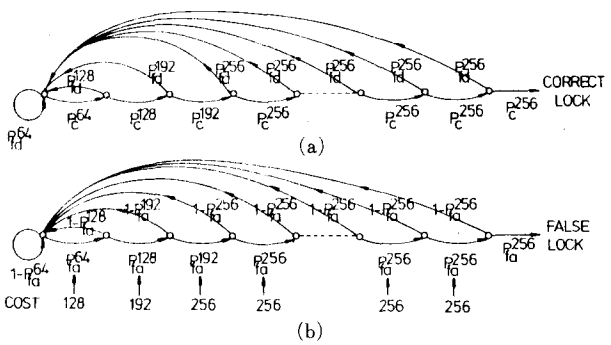

Fig. 3. State transition diagram.
(a) when synchronization occurs.
(b) when synchronization does not occur.

$$C_{fa1} = 128\ P_{fa}^{64}(1 - P_{fa}^{128}), \tag{6}$$

and in the second stage it is

$$C_{fa2} = (128+192)\, P_{fa}^{64} P_{fa}^{128} (1-P_{fa}^{192}).$$

Since we verify ten times in the last verification stage, we have

$$C_{fa3} = \sum_{\ell=1}^{10} (128+192+256\ell)\, P_{fa}^{64} P_{fa}^{128} P_{fa}^{192} (P_{fa}^{256})^{\ell-1} (1-P_{fa}^{256}). \tag{7}$$

Hence, the total cost function of false alarm becomes

$$C_{fa} = 64[2P_{fa}^{64}(1-P_{fa}^{128}) + 5P_{fa}^{64} P_{fa}^{128}(1-P_{fa}^{192}) + \sum_{\ell=1}^{10} (5+4\ell)\, P_{fa}^{64} P_{fa}^{128} P_{fa}^{192} (P_{fa}^{256})^{\ell-1} (1-P_{fa}^{256})]. \tag{8}$$

The cost function of false dismissal can also be derived similarly. The resulting total cost function of false dismissal becomes

$$C_{fd} = 64[2P_c^{64}(1-P_c^{128}) + 5P_c^{64} P_c^{128}(1-P_c^{192}) + \sum_{\ell=1}^{10} (5+4\ell) P_c^{64} P_c^{128} P_c^{192} (P_c^{256})^{\ell-1} (1-P_c^{256})], \tag{9a}$$

or using (5) we have

$$C_{fd} = 64[2P_c^{64} P_{fd}^{128} + 5P_c^{64} P_c^{128} P_{fd}^{192} + \sum_{\ell=1}^{10} (5+4\ell) P_c^{64} P_c^{128} P_c^{192} (P_c^{256})^{\ell-1} (1-P_c^{256})], \tag{9b}$$

The probability of correct lock, i.e., the probability that the retained phase of local PN sequence at the end of verification is correct, can be derived from the state transition diagram of Fig. 3 and (5) as

$$P_{cl} = P_c^{64} P_c^{128} P_c^{192} (P_c^{256})^{10}. \tag{10}$$

Then, $1/P_{cl}$ becomes an average number to be tested to give a final decision as correct synchronization without false dismissal in any verification stage. Since, once a false dismissal occurs, one must slide the amount of the entire PN sequence period to have another opportunity of correct lock, the average number of bit intervals to slide to find correct synchronization is

$$N_c = \frac{1}{P_{cl}} (2^n - 1) \tag{11}$$

where n is the number of shift register stages of the PN sequence generator. Also, the total average number N_f of bit intervals for which slide does not occur due to false alarm in the initial synchronization processes is

$$N_f = N_c \cdot C_{fa}. \tag{12}$$

Other factors to be considered for exact expression of acquisition time are cost of false dismissal and minimum time that is inherent in the proposed system. The average number of occurrence of false dismissal during PN sequence acquisition is

$$N_{fd} = \frac{1}{P_{cl}} - 1. \tag{13}$$

Hence, the average number of bit time intervals used due to false dismissal is given by

$$N_d = N_{fd} \cdot C_{fd}. \tag{14}$$

And the total bit time intervals required for final verification of synchronization are equal to the sum of correlation length in each verifi-

cation stage. Also, since we can assume that the initial phase offset between the incoming signal and the local PN sequence is one half of the PN sequence period, we must subtract the amount from (11) in which the total length of the sequence is assumed. Therefore, the total average bit time intervals needed to find correct synchronization becomes

$$N_{acq} = N_c + N_f + N_d + (128+192+2560) - \left(\frac{2^n - 1}{2}\right) \tag{15}$$
$$= \frac{1}{P_{cl}}(2^n - 1)(1+C_{fa}) + \left(\frac{1}{P_{c\ell}} - 1\right) C_{fd} + 2880 - \left(\frac{2^n - 1}{2}\right).$$

Accordingly, average acquisition time can be expressed as

$$T_{acq} = N_{acq} \cdot \triangle \tag{16}$$

where $\triangle$ is one bit interval of PN sequence.

Another important parameter to be considered is probability of false lock. The successive occurrence of false alarm in every verification stage results in a false lock. Hence, if we note that the false lock can occur in every verification step and that the total number of bits to be slided during the entire PN sequence acquisition period is N_c, the probability of false lock can be written as

$$P_{fl} = P_{fa}^{64} P_{fa}^{128} P_{fa}^{192} (P_{fa}^{256})^{10} N_c. \tag{17}$$

Then, we must decide the threshold of each stage that can minimize the acquisition time and the false lock probability simultaneously. Since there is no way of finding a unique optimum threshold analytically, we must use a rule of thumb criterion.

In selecting the optimum threshold that minimizes the acquisition time given by (16), we assume additive white Gaussian noise (AWGN) as the only source of estimation error.[2] Also, we minimize the acquisition time at the SNR of -18 dB that is the lower limit of our system design goal. [3]

To find the probability of estimation error, we assume that noise n(t) is zero-mean white Gaussian with spectral density N_o and the transmitted signal is

$$s(t) = +1 \text{ when one is transmitted}$$
$$= -1 \text{ when zero is transmitted.}$$

Then, the signal at the input of the estimator can be written as

$$r(t) = \sqrt{E}s(t) + n(t) \tag{18}$$

where E represents energy of the signal. Since we can assume that the number of transmitted 0's is equal to the number of 1's, by the optimum decision rule [5] we have

$$s'(t) = +1 \quad \text{when } r(t) \geq 0$$
$$= -1 \quad \text{when } r(t) < 0$$

where S'(t) is the estimated signal.
Therefore, the probability of estimation error can be written as [6]

$$P = \frac{1}{\sqrt{2\pi}} \int_{\sqrt{\frac{E}{N_o}}}^{\infty} e^{-v^2} \, dv. \tag{19}$$

With the probability of estimation error at the SNR of -18 dB, we can compute the acquisition time for various threshold values of search stage.

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2 In addition to white Gaussian noise, there are other disturbances such as jamming and multipath interference. The effect of jamming on the performance of our acquisition system is presently being investigated.

3 Hence, we minimize the maximum acquisition time.

IV. Computer Simulation and Comparison of Results

The proposed PN squence acquisition algorithm has been simulated on a minicomputer. In the simulation, we used a 10 stage m-sequence generator and the code rate of 5 Mbits/s. To simulate the effect of channel noise and jamming, we modeled the channel as shown in Fig. 4. Since the tracking system, which keeps precise synchronization, has a resolution of $\triangle/15$, the generated PN sequence must be up-sampled by a factor of 15. Consequently, the noise and jamming must be generated at 75 MHz because the rate of the PN sequence is 5 Mbits/s. Therefore, the rate of the up-sampled signal is 75 Mbits/s.

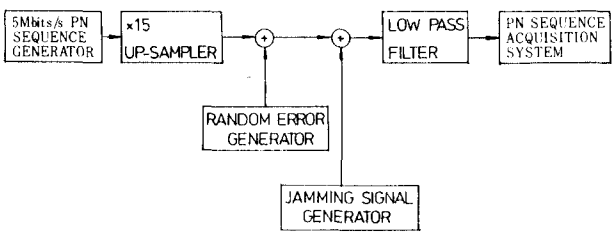

Fig. 4. Block diagram of computer simulation model.

The noise has been generated by Gaussian noise generator program at the rate that is the same as that of the up-sampled transmitted signal. Therefore, the bandwidth of noise can be assumed to be 75 MHz. And, since the bandwidth of the wideband filter is 5 MHz, noise power after filtering becomes

$$P_N = \frac{5}{75}\ \sigma^2 \qquad (20)$$

where σ^2 is variance of white Gaussian noise. Hence, the input SNR of the estimator can be written as

$$\text{SNR} = 10 \log \frac{15E}{\sigma^2}\ [\text{dB}]\ . \qquad (21)$$

The low-pass filter (LPF) used is a 135-tap finite impulse response (FIR) digital filter with cutoff frequency at 5 MHz. Therefore, the computer must compute 15 x 135 multiplications for 1 bit estimate. Since the average number of estimates required for initial synchronization is about 200,000 for low SNR, the average number of multiplications required for PN sequence acquisition in simulation was about 4 x 10^8. Furthermore, to acquire the statistical average of the acquisition time, the simulation must be carried out at least hundreds times. This amount of computation makes it impossible to simulate the system on the minicomputer. To overcome the limitation, we used several approaches that can reduce computations. In digital filtering, we computed only the required 2 samples (in the search stage) or 1 sample (in the verification stage) out of 15 input samples. By this approach, the number of multiplications could be reduced by a factor of 2/15 or 1/15. Nevertheless, the number of multiplications was still too large to simulate by the minicomputer. Therefore, we simulated average cost of false alarm and correct lock probability rather than having direct simulation of the proposed acquisition system.

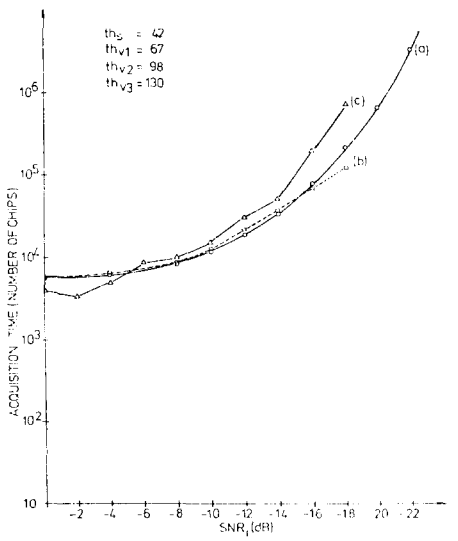

Fig. 5. Comparison of average acquisition time vs. SNR of (a) analytic result, (b) simulation result, and (c) hardware test result.

With the simulated average cost of false alarm and correct lock probability, we calculated average acquisition time using (15) and (16). With this technique, we did not have to simulate the initial synchronization process hundreds times for statistical averaging of the acquisition time.

A comparison of average acquisition time obtained by various methods is shown in Fig. 5. As seen in the figure, the analytical result agrees closely with the simulation and hardware test results.

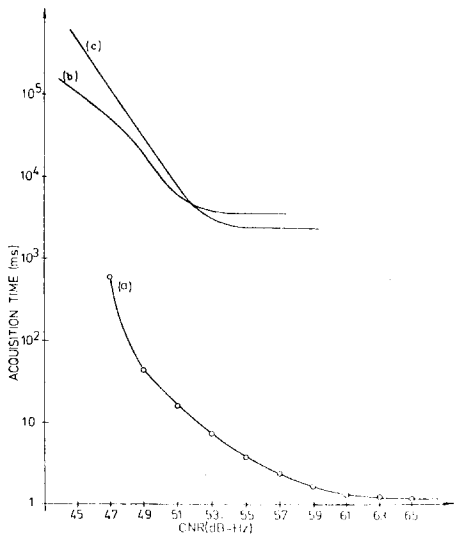

Fig. 6. Comparison of average acquisition time of (a) the proposed system and analog sliding correlators of (b) Hopkins and (c) Eisenberg and Sheppard.

In Fig. 6 we compare the acquisition time of the proposed system with those of conventional analog sliding correlators. Since the given conditions of the two systems (e.g., information bandwidth, PN chip rate and length of the PN sequence) are different, one should not regard this comparison as a fair one. Nevertheless, one can draw a conclusion easily that the proposed system requires far less acquisition time than the conventional sliding correlators. According to the analysis results of Hopkins [7], Cobb and Osborne [8] and Eisenberg and Sheppard [9], acquisition time of the conventional system requires a few seconds to hundreds seconds which is much longer than that of the proposed system. In Fig. 6 we have used carrier-to-noise ratio (CNR) rather than SNR for convenience, which is defined by

$$\text{CNR (dB-Hz)} = 10 \log \frac{E}{N_0} \tag{22}$$

where E and N_0 denote signal power and noise spectral density, respectively. The relation between CNR and SNR is given by

$$\text{CNR} = \text{SNR} + 10 \log B \tag{23}$$

where B denotes the bandwidth of the input wideband filter. Since the bandwidth is 5 MHz in the proposed system, the relation can be written as

$$\text{CNR} = \text{SNR} + 67.$$

V. Hardware Implementation

The proposed PN sequence acquisition algorithm has been implemented in a spread spectrum communication system. In the developed acquisition system, a Cromemco Z-80 single card computer (SCC) was used to control the acquisition hardware, and two TRW 64-bit digital correlators have been used for real time digital correlation.

Since the proposed PN acquisition system operates at 5 MHz that is much faster than the control speed of Z-80 SCC, real time control of the hardware is not possible. Therefore, most of the proposed algorithm has been implemented in hardware, and the SCC has been used only for the control of correlation length and threshold.

A block diagram of the implemented hardware is shown in Fig. 7. In the hardware, the signal from the RF demodulator is filtered and converted into a 1-bit binary sequence by an estimator. The estimator samples the filtered signal in every one half chip interval and outputs even and odd samples separately

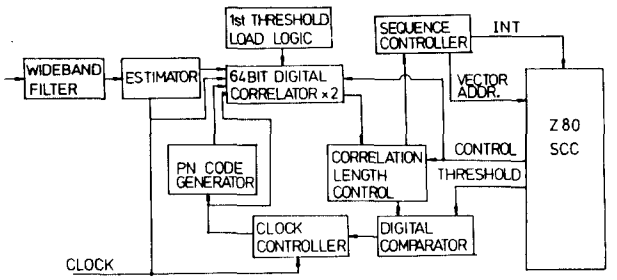

Fig. 7. Block diagram of the developed PN sequence acquisition system.

during the search process. Each estimated sequence is then fed into two correlators which are connected in parallel during the search process. In the search process, the clock controller disables the clock of the PN sequence generator to slide the phase of the incoming signal with respect to that of the local PN sequence. In the search mode, the threshold register and the digital comparator in each correlator are used.

When any of the correlation values exceeds the threshold of the search stage, the clock controller enables the clock of the PN sequence generator, and the correlation length controller connects two correlators in series for longer correlation. In addition, an adder is used to add the correlation results of each correlator, and an external digital comparator is used to test correlation results in the verification stage. Unlike the search stage, the threshold in each verification stage is supplied by the SCC.

To track the end of each verification stage and to detetmine the time when the correlation value must be added, two presettable binary counters are employed. Since the SCC is much slower than the counter, loading a preset value to the presettable counter is done during the preceding stage. That is, the preset value of the first verification stage is loaded during the search stage, and the preset value of the second verification stage is loaded during the first verification stage and so on. Hence, the processor must keep track of hardware status to provide proper control signals and threshold value for the hardware. For this purpose, the vectored interrupt, interrupt mode-2 of Z-80 microprocessor, is used. Every time the hardware changes its status, the interrupt is generated with vector address that indicates the starting address of control program for that stage.

VI. Conclusions

In this work a digital correlation method of PN sequence acquisition has been investigated. To evaluate the performance of the developed algorithm, analysis on the acquisition system has been done. Also, computer simulation has been carried out for various input SNR's. Then, the performance of the proposed system has been compared with those of RASE and RARASE systems of Ward and various analog sliding correlators. It can be concluded that the proposed PN sequence acquisition system yields better performance when the input SNR is low than the systems so far studied. In addition, the proposed PN sequence acquisition algorithm has been realized using the latest TRW digital correlator and Cromemco Z-80 SCC. The acquisition time obtained from hardware test agree closely with the analysis and simulation results.

The newly developed acquisiton system is particularly advantageous in that, unlike other systems which take at least a few seconds of acquisiton time, it takes only 45 ms at most when SNR is -18 dB. Hence, the system can be used practically in the DS spread spectrum voice tranceiver that requires less than 300 ms of acquisition time.

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