Design and Process of Vertical Double Diffused Power MOSFET Devices

(二重擴散 方法에 依한 垂直構造形 電力用 MOSFET의 設計 및 工程)

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要 約

이중확산공정에 의한 수직구조의 전력 MOSFET (VDMOS)를 설계 및 제작하고 그 성능에 대하여 기술하였다. 안티몬 (Sb)이 약 7×10^{17} cm^{-3} 도우핑된 초기 실리콘기판(N^+) 위에 비저항 약 12Ω-cm, 두께 32μm의 에피층(N^-)을 성장시켰다. 폭 21μm의 폴리실리콘에 의해 P^- 및 N^+ 확산공정을 자기정렬(self align) 방식으로 수행하여 게이트 및 소오스를 형성하였고, 이때 P^-채널 길이를 1~2μm 정도로 조정하였다. 도통저항(on-resistance, R_{on})을 1Ω정도 유지시키면서 소자의 항복전압을 증가시키기 위하여 세겹의 P^+ 확산띠 (guard ring)를 칩 주변에 배치하였다. 칩 면적 4800μm×4840μm인 전력 MOSFET는 항복전압 410~440V, 허용전류 5A이상, R_{on} 1.0~1.2Ω의 특성을 보였다.

Abstract

The design, fabrication and performance of a vertical double diffused power MOSFET (VDMOS) were described. On the antimony (Sb) doped (~7×10^{17} cm^{-3}) silicon substrate (N^+), epitaxial layer (N^-) was grown. The thickness and the resistivity of this layer were 32μm and about 12Ω-cm, respectively. The P^- channel length which was controlled by sequential P^-/N^+ double diffusion method was about 1~2 μm, and was processed with the self alignment of 21 μm width poly silicon. To improve the breakdown voltage with constant on-resistance (R_{on}) about 1Ω, three P^+ guard rings were laid out around main pattern. With chip size of 4800 μm x 4840 μm, the VDMOS has shown breakdown voltage of 410~440 V, on- resistance within 1.0~1.2Ω and the current capability of more than 5A.

I. Introduction

Until recently, silicon bipolar transistor is the major active components of medium to high frequency power amplification and switching applications due to a high average chip current density and good geometrical control of the active transit region width [1,2].

However, field effect transistors (FET's) offer several attractive features as high power devices[3-7]. First, these devices have a high switching speed due to the absence of minority carrier storage effect. Second, these devices

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have a higher input impedance than bipolar transistors, which greatly simplifies the gate drive circuit. In addition, the negative temperature coefficient of the drain current in these devices allow their operation to be in parallel without the thermal runaway problem that is prevalent in bipolar transistors. Further, since these transistors are majority carrier devices, the processing of these devices dose not require the stringent controls on the minority carrier lifetime that is necessary during the fabrication of bipolar transistors. These superior capabilities has arisen primarily through the use of double diffusion techniques to achieve short active channels and the incorporation of a lightly doped drift region between the channel and the drain contact, which largely supports the applied voltage.

Many different structures have been proposed to implement these new devices such as the lateral double diffused transistor (LDMOS), the vertical double diffused transistor (VDMOS), and the V-groove double diffused transistor (VMOS). The three DMOS structures are shown in cross section in Fig. 1.

The choice of (100) material for LDMOS and VDMOS provides the improvement in electron inversion layer mobility and electron scattering limited velocity. These effects result in lower channel resistance and higher device transconductance per unit width in the LDMOS and VDMOS structures. The VMOS is constrained to have its channel along an etched (111) surface[8]. For this reason, VMOS may itself brings on higher Q_f that causes impact on other device parameters such as noise performance in linear amplifications. Other disadvantages of the nonplanar device are the fabrication difficulties in terms of metal coverage and photolithography. On the otherside, the VMOS and VDMOS structures require only two of the electrodes on the top surface. This would tend to indicate that they should be capable of higher packing density than the LDMOS which has the drain connection on the top surface[9]. Taking these effects into consideration, VDMOS has been adapted to be the best for achieving high breakdown voltages as well as high current handling capability.

This paper describes the VDMOS power transistor using silicon gate MOS IC technology. The design and the process parameters are optimized to provide 410~440V drain-source breakdown voltage with more than 5 A drain current and 1.0~1.2Ω on-resistance.

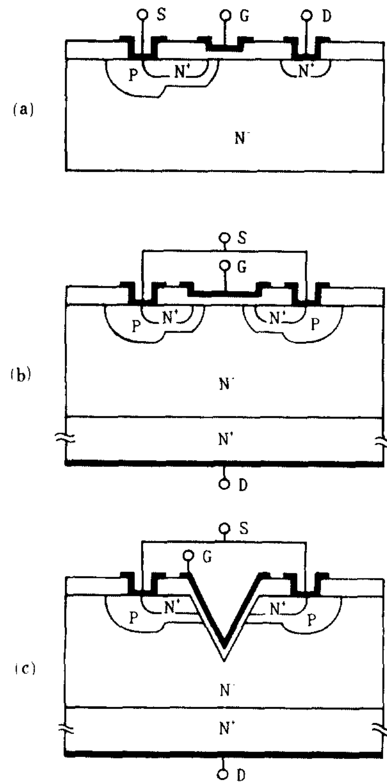


Fig. 1. Cross sections of three high voltage DMOS devices.
(a) LDMOS,
(b) VDMOS,
(c) VMOS.

II. Design and Fabrication

1. Design Considerations

The N^- epi-layer should be so much thick and high-resistive to be depleted far enough before avalanch breakdown occurs. That is for advancing the source-drain breakdown voltage. The source is shorted to P-well. However, too much thick and high-resistive N^- epi-layer also raises on-resistance, R_{on}. For these reasons the most important design

trade-off for power MOSFET's is that between on-resistance and breakdown voltage.

A proper design procedure of the power MOSFET and the minimization of the ideal N^- epitaxial layer resistance for a given desired breakdown voltage V_B (100~1000V range) have been discussed by C. Hu et al.[10]. Assuming a uniform doping level in the N^- epi-layer, the optimum thickness W, and the resistivity ρ are

$$W = 1.74 \times 10^{-6} \times V_B^{1.2} \text{ cm} \quad (1)$$

$$\rho = 4.55 \times 10^{-3} \times V_B^{1.3} \ \Omega\cdot\text{cm}. \quad (2)$$

Using (1) and (2) we chose W and ρ as 25.5 μm and 12 Ω-cm respectively to obtain 400 V breakdown characteristics with 10% safety margin.

The on-resistance R_{on} is determined by a series combination of several elements (Fig. 2-(a))[10]. For a high voltage device, the largest contribution to R_{on} is the resistance of the epitaxial layer below the gate

$$R_{epi} = R_{ideal}\cdot\gamma_{epi} = \rho\cdot\frac{W}{A}\gamma_{epi} \quad (3)$$

where A is the total active device area, γ_{epi} is the spreading resistance factor. γ_{epi} has been estimated with 45° spreading-angle model for linear geometry[10].

JFET resistance (R_j) was considered as the second element of R_{on} by the presence of parasitic JFET between adjacent P wells as shown in Fig. 2-(b). A trapezoid model is used for the calculation of R_j. If the depletion region width is negligible compared to well spacing, R_j can be predicted as

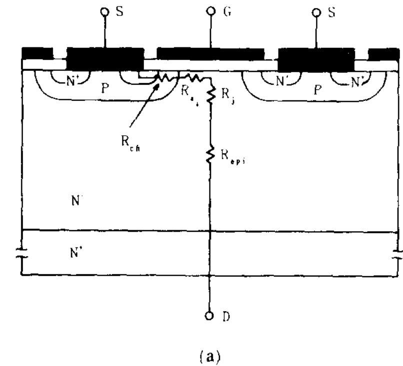
$$R_j = \frac{\rho\cdot W_j}{a/(s+a)}\ \frac{1}{A} \quad (4)$$

where W_j is the junction depth of the well and s is the well width. When the ratio of neck area to cell area is less than 40%, the other elements are much smaller than $R_{epi} + R_j$. The total on-resistance can be written

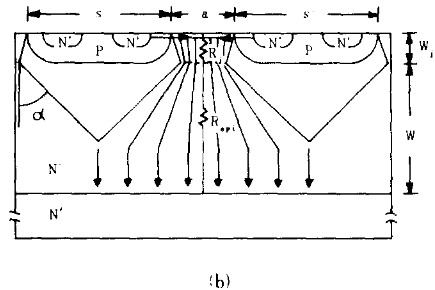
$$R_{on} \simeq R_{epi} + R_j \quad (5)$$

To meet fabrication compatibility and minimization of R_{on} (<1Ω) with fixed ρ and W, we chose the ratio of neck area to cell area as 30%. Design rules for the device was 6μm minimum feature sizes and 2μm alignment tolerances. Considering that lateral diffusion length is 4μm by double diffusion technology, we set poly width and poly to poly distance all 21μm. This paper adapted the stripe cell geometry which has 7μm x 7μm contact size.

To improve the breakdown voltage with constant on-resistance, P^+ guard rings were applied around the active region[11]. Three guard rings were each apart from active region 20μm, 50μm, 84μm, respectively, and their widths were all the same as 10μm. The edge of the 3rd guard ring was surrounded by equipotential metal line for channel stopping which has gap as 34μm.



(a)



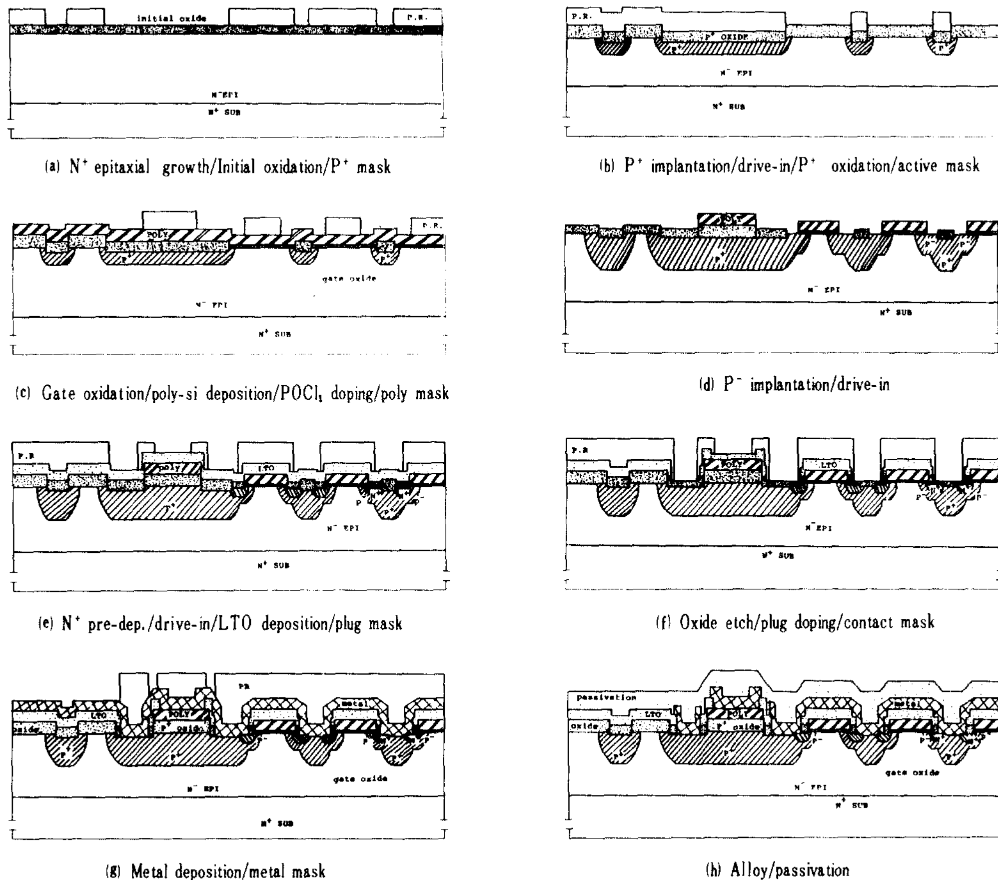
(b)

Fig. 2. (a) The four components of on resistance are shown for a power VDMOS transistor.
(b) Definition of R_j and R_{epi}. Current is assumed to flow within α° spreading-angle. The narrowest part is the neck of the JFET.

2. Device Fabrication

In Fig. 3, the VDMOS fabrication steps are shown. Highly doped Sb (~7 x 10^{17} cm^{-3}), N^+ substrates were used; the N^- layers were grown with conventional epitaxial techniques. The thickness and the resistivity of the epitaxial layer were approximately 32μm and 12Ω-cm respectively.

An initial SiO_2 film was grown with 2000 A thickness (Fig. 3-(a)). After delineating the P^+ region and etching away the film, boron implantation of 3 x 10^{14} cm^{-2} dose was performed using 100 KeV energy. The drive-in for the boron and P^+ doped oxide growing were carried at 1150°C for 60 minutes in N_2 gas and at 950°C for 150 minutes in wet O_2 ambient respectively. The resulting P^+ oxide thickness was 5000Å (Fig. 3-(b)). And then defining of the active region, gate oxidation, poly silicon deposition and poly doping process were followed. The gate oxide was thermally grown to a thickness of 1500 Å using C_2HCl_3/O_2 ambient at 1000°C for 200 minutes. Poly silicon deposited at 625°C with 5500 Å thickness, was doped with phosphorus under $POCl_3$ at 950°C (Fig. 3-(c)). After delineating poly silicon gate by dry etching, boron implantation (P^- implantation) and gate oxide layer etching were carried successively. P^- implantation was processed by 1 x 10^{14} cm^{-2} of boron using 80 KeV energy. P^- diffusion was performed at 1150°C for 720 minutes. The P^- oxide was grown to a thickness of 1500 Å (Fig. 3-(d)). Removing P^- oxide carefully, N^+ predeposition was followed under 900°C in $POCl_3/O_2$ ambients for 10 minutes and in N_2 gas for 10 minutes sequentially. N^+ oxidation and drive-in were performed with 925°C, O_2 ambient for 30 minutes. These P^-/N^+ double diffusion



(a) N^+ epitaxial growth/Initial oxidation/P^+ mask

(b) P^+ implantation/drive-in/P^+ oxidation/active mask

(c) Gate oxidation/poly-si deposition/$POCl_3$ doping/poly mask

(d) P^- implantation/drive-in

(e) N^+ pre-dep./drive-in/LTO deposition/plug mask

(f) Oxide etch/plug doping/contact mask

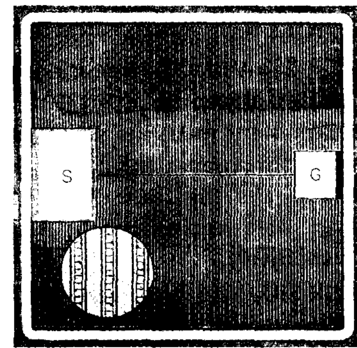
(g) Metal deposition/metal mask

(h) Alloy/passivation

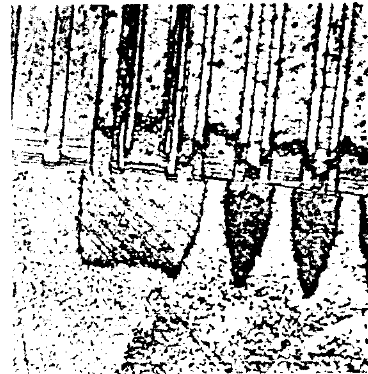
Fig. 3. Processing steps for VDMOS.

processes are key steps to control the channel length, threshold voltage stability, and P^+/P^- junction depth. The difference in lateral diffusion between the P^- and N^+ regions forms a controllable 1 to 2 μm channel length along the surface. The sequential diffusion processes made the final vertical junction depth of P^+, P^- and N^+ as 6.5 μm, 4 μm and 2.5 μm, respectively. After depositing 6000Å thickness of SiO_2 which has 8% phosphorus concentration, PSG flowing was performed at 925°C, H_2/O_2 ambient (Fig. 3-(e)). The PSG film and underlying N^+ oxide were etched out carefully. For reducing N^+ source to metal contact resistance, plug doping process was carried at 1000°C with $POCl_3/O_2$ ambient (Fig. 3-(f)). After etching the plug and P^+ oxide successively, 2% Si-Al alloy was sputtered for the gate and source electrodes (Fig. 3-(g)). Silicon nitride film was deposited by PECVD as passivation layer (Fig. 3-(h)). For back side (drain) metallization, Cu-Zn alloy was used.

A surface photomicrograph of the completed device structure is shown in Fig. 4-(a). A cross section of the device after angle lapping and junction delineation is shown in Fig. 4-(b). Gate and source pad area were 680 μm x 720 μm and 900 μm x 1280 μm respectively. The chip area including guard ring was 4800 μm x 4840 μm, and was assembled in T0-220 and T0-3 package.



(a)



(b)

Fig. 4. (a) Photograph of the VDMOS power transistor.
(b) Photograph of device cross section delineated by angle lapping and junction staining techniques.

III. Results and discussions

1. Breakdown and on-resistance characteristics

Resistivity and thickness of the epi-layer was measured by C-V plot method and film thickness gauge (FTG), respectively. The breakdown voltage and on-resistance characteristics of this device were compared with the values expected from (3), (4) and (5) (Table 1). The active area (A) excluding guard rings and bonding pads is 16.4 mm^2. The well junction depth (W_j), well width (s) and well spacing (a) are 6.5 μm, 29 μm and 13 μm respectively.

Table 1. Comparision of some experimental breakdown and on-resistance characteristics with expected value.

T_{epi} *1 (μm)	ρ_{epi} (Ω-cm)	BV (V)	R_{on} (Ω)	R_{epi} *2 (Ω)	R_j *2 (Ω)	R_{on} *2 (Ω)
27.6	19	380	1.9	0.37	0.24	0.61
27.7	14	380	1.3	0.27	0.18	0.45
29.3	14	380	1.4	0.29	0.18	0.47
27.2	15	380	1.5	0.28	0.19	0.47
32.2	12	430	1.1	0.29	0.15	0.44
25.0	6	310	0.5	0.10	0.08	0.18

* 1 : T_{epi} = W + W
* 2 : Expected value from (3), (4) and (5)

As shown in table 1, on resistances of devices have about 2 ~ 3 times higher than theoretical values. The reasons for this differences may come from the unstabilities of fabrication process such as the epitaxial layer growth, P^- double diffusion, and so on.

2. Guard Ring Effect on Breakdown Voltage

In Fig. 5, the breakdown voltage of the guard ring structure has shown to be a relatively sensitive function of the seperation between the main junction and the guard ring. Guard ring spaces were varied from 10 μm to 80 μm with 0.010 ~ 0.015 Ω–cm of substrate resistivities.

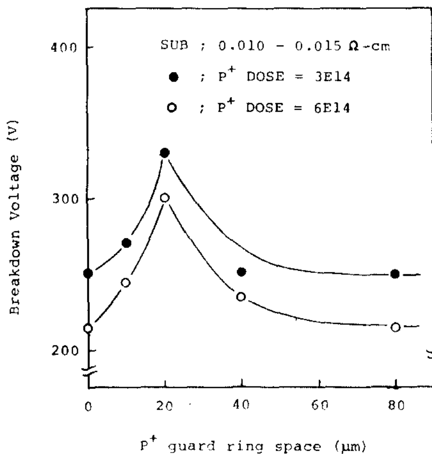


Fig. 5. Breakdown voltage vs guard ring space.

For this substrate, 3 x 10^{14} cm^{-2} and 6 x 10^{14} cm^{-2} of boron were implanted with 100 KeV energy. In fact, these guard rings are made at P^+ diffusion process. Within the ranges of implant dose and sheet resistance, the optimum guard ring space was 20 μm. Compared with no guard ring function, the guard ring structure having 20 μm space showed the improvement of about 30 to 40 percent in breakdown voltage. Using this result, three guard rings were adapted in main chip. The space distances between junctions were 20 μm, 20 μm and 24 μm, respectively.

The reason of multi guard ring is illustrated in Fig. 6 [1].
The depletion layer is initially associated with the main junction P_0, and extends outward with increasing reverse bias. The spacing between P_0 and P_1 is such that punch through occurs before the avalanche breakdown voltage of the cylindrical junction associated with P_0. Thus the maximum electric field across the main junction P_0 is limited, any further increase in reverse voltage is taken up by P_1 until

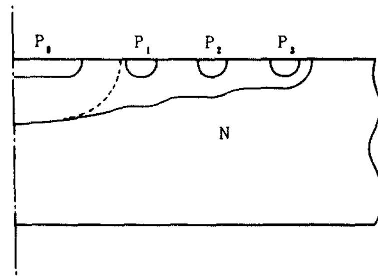


Fig. 6. Diffused field-limiting ring.

the depletion layer punches through to P_2, and so on. Ultimately, the device breakdown at cylindrical junction is associated with the last diffused ring. To avoid excessively large chip area, practical number was limited to three guard rings. A test chip which has 200 times reduced active area with a combination of three guard rings and metal equipotential ring is shown in Fig. 7. Metal equipotential ring was set for the improvement of the device reliability.

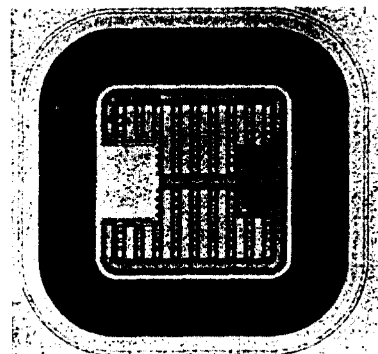
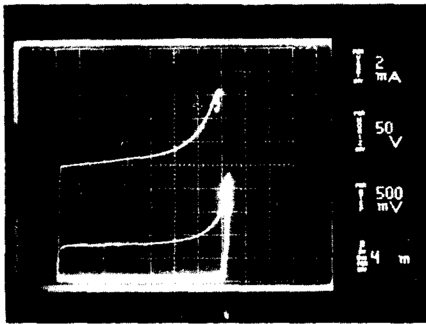


Fig. 7. A full photograph of reduced test chip with three guard rings and metal equipotential ring.

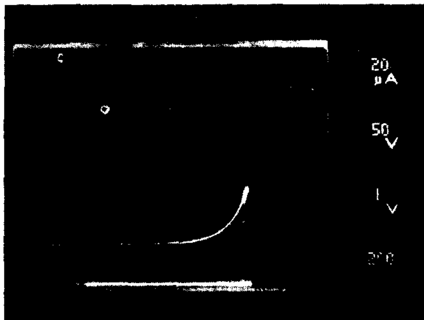
Fig. 8-(a) and (b) show the breakdown characteristics of the test chip. Compared with no-guard-ring device (Fig. 8-(a)), three-guard-ring device (Fig. 8-(b)) has 30 percent increase of breakdown voltage. As shown in Fig. 8-(b), 430 V of breakdown voltage could be obtained.

3. Main Chip Characteristics

Fig. 9-(a) and (b) show the linear and

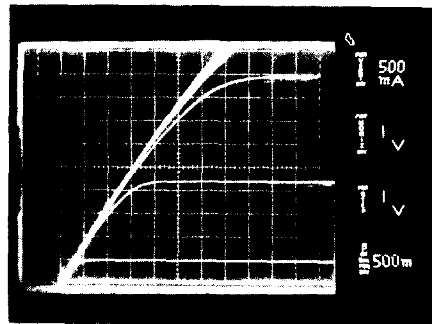


(a)

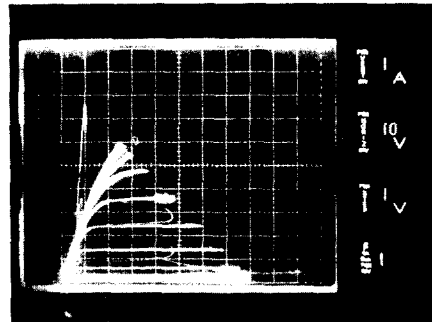


(b)

Fig. 8. Breakdown characteristics of test chip;
(a) no-guardring.
(b) combination of three-guard-rings and metal equipotential ring.



(a)



(b)

Fig. 9. (a) Linear.
(b) Saturation characteristics of main chip.

saturation characteristics of main chip.

From Fig. 9-(a), it can be seen that on-resitance (R_{on}) is 1.1 Ω. The threshold voltage $V_{gs(th)}$ is defined as the gate-source bias required for a drain-source current of 1 mA. The summary of the power MOSFET parameters was listed in Table 2.

Shown in Fig. 10 is the switching test circuit and response of the device in a T0-220 package. With a 10 V, 200 μs pulse applied to the plate, the characteristics shown in Fig. 9-(b) are measured at the output. Turn-on delay, rise, turn-off delay and fall time were 60 ns, 40 ns, 100 ns, respectively.

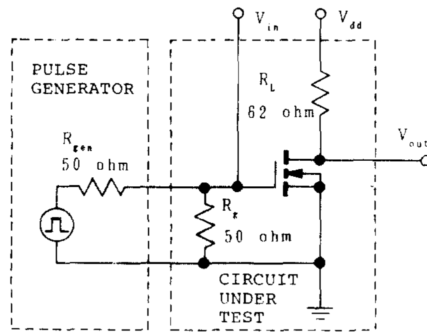
Table 2. VDMOS electrical data and test conditions.

Code;PM07 #09. Package;TO-220

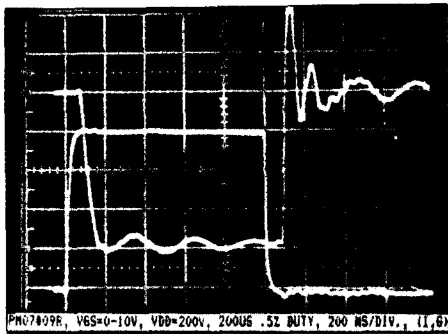
ELECTRICAL CHARACTERISTICS			
Parameter	Measurement	Unit	Test Conditions
BV_{dss}	410~440	V	$V_{gs}=0$, $I_d=1mA$
$V_{gs}(th)$	4.0~4.2	V	$V_{gs}=V_{ds}$, $I_d=1mA$
$R_{ds}(on)$	1.0~1.2	ohm	$V_{gs}=10V$, $I_d=2.5A$, pulse test
$I_d(on)$	>5	A	$V_{gs}=10V$, $V_{ds}=10V$
g(fs)	3.0	A/V	$V_{ds}=10V$, $I_d=2.0A$, pulse test
C_{in}	2000	pf	$V_{gs}=0$, $V_{ds}=25V$, f=1MHz
$t_d(on)$	60	ns	$V_{dd}=200V$
t_r (rise)	40	ns	$V_{gs}=0$ to 10V pulse test (200μs, 0.5% duty cycle)
$t_d(off)$	100	ns	$R_L=62ohm$, $R_{gen}=50ohm$
t_f (fall)	50	ns	I_d about 3 A

IV. Conclusion

The design, fabrication, and device measurements for a high voltage vertical double diffusedMOSFET have been discussed.The process was that N^-/N^+ epitaxial wafer was used as the



(a)



(b)

Fig. 10. Illustration of the dynamic switching capability of the VDMOS transistor
(a) Test circuit.
(b) Output response.

starting material and P^-/N^+ double diffusion was involved, simultaneously forming P^+ guard rings around the chip. Using these techniques and 12 Ω–cm, 32 μm thick N^- epi-layer, drain breakdown voltage as high as 430 V, on-resistance as low as 1.1 Ω and current capability more than 5 A were achieved within an area of 4800 μm x 4840 μm.

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