Layer Assignment of Functional Chip Blocks for 3-D Hybrid IC Planning

(3 차원 Hybrid IC 배치를 위한 기능칩 블록의 층 할당)

李 坪 漢*, 慶 宗 旻*

(Pyong-Han Lee and Chong-Min Kyung)

要 約

종래의 cluster 형성을 통한 회로 분할 알고리즘은 I/O 연결 핀내에 cluster간의 연결 net가 놓여 있는 칩평면 계획 문제나 여러 장의 PCB 시스템 배치 문제에 적합하지만, 진정한 3 차원 구조의 전자모듈내의 기능블록 배치 문제에는 적합치 못할 수 있다. 3 차원 hybrid IC는 층 내의 배선뿐 아니라 층간의 배선을 최대한 활용함으로써 전체 회로체적, 냉각부하를 줄이고, 동작속도를 향상시킴을 목적으로 하는 문제의 좋은 예이다. 이 논문에서는 3 차원 hybrid IC 설계에서 각 기능블록의 층 할당을 위한 MBE (minimum box embedding) 라는 알고리즘을 제안한다. MBE 알고리즘은 i) 3 차원 공간상의 FDR(force-directed relaxation), ii) 층 분할 평면의 최적 방향을 찾는 것과 iii) 층 할당의 순서로 수행된다. 우선 2 차원 공간상의 축소된 문제에 대하여 이 알고리즘을 설명하고, 3 차원 경우에 확장하였고, 80개의 블록으로 이루어진 회로에 대한 수행 예를 보였다.

Abstract

Traditional circuit partitioning algorithm using the cluster development method, which is suitable for such applications as single chip floor planning or multiple layer PCB system placement, where the clusters are formed so that inter-cluster nets are localized within the I/O connector pins, may not be appropriate for the functional block placement in truly 3-D electronic modules. 3-D hybrid IC is one such example where the inter-layer routing as well as the intra-layer routing can be maximally incorporated to reduce the overall circuit size, cooling requirements and to improve the speed performance. In this paper, we propose a new algorithm called MBE (Minimum Box Embedding) for the layer assignment of each functional block in 3-D hybrid IC design. The sequence of MBE is as follows; i) force-directed relaxation in 3-D space, ii) exhaustive search for the optimal orientation of the slicing plane and iii) layer assignment. The algorithm is first explained for a 2-D reduced problem, and then extended for 3-D applications. An example result for a circuit consisting of 80 blocks has been shown.

1. Introduction

Despite the impressive progress being made in the VLSI technology and the design area, there still exist some limits in the number of gate counts, chip area and functionality achievable within a single VLSI chip. Wafer-scale integration and 3-dimensional IC are now being actively investigated as a future technology to seek a breakthrough in these aspects.

*正會員, 韓國科學技術院 電氣 및 電子工學科

(Dep. of Elec. Eng., KAIST)

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On the other hand, the 3-dimensional hybrid IC (3-D HIC) is expected to play a significant role in reducing overall circuit volume, package counts, cooling requirements, and improving the circuit speed, especially for the applications such as space, aircraft and military electronics. 3-D HIC is different from the multiple layer PCB not only in that IC chips are mounted unpackaged but that the active components as well as the interconnections can be dispersed over all layers thereby significantly reducing the final module size with the upgraded speed performance.

In this paper, we will describe an automatic layer assignment procedure as a preprocessing step for the whole 3-D HIC placement planning, where the inter-layer routing as well as the intra-layer routing needs to be intensively exploited to achieve fast speed and compact packaging. Conventional circuit partitioning approach using the cluster development method is only appropriate for such applications as chip floor planning or multiple layer PCB system design, where the number of interconnection nets between clusters (circuit blocks in VLSI chip floor plan, or one layer in multiple layer PCB system) is assumed to be relatively small. In other words, conventional partitioning algorithms[1] are aimed at reducing the number of I/O pins at the localized connector bus.

A sketch of 3-D HIC realized by the layer assignment and the placement of the functional VLSI chips, followed by the inter - and the intra-layer routing is shown in Fig.1. Here, strong correlation generally exists among the placement configurations on each layer, which makes it a 3-D rather than 2-D placement problem. On the other hand, various chip floor planning algorithms have been reported including the building block layout[2], the dual graph method[3], the force-directed relaxation [4], and the channel position graph method [5]. Most of these methods are basically oriented toward layout in 2-D plane, and do not easily lend themselves to 3-D extension for 3-D HIC placement planning.

In our algorithm called MBE (Minimal Box Embedding), the center-of-mass (CM) positions of each functional block are first distributed in 3-dimensional space according to the traditional force-directed relaxation method [4]. These CM-points are to be allocated to each layer according to the constraints that the whole circuit should be embedded in the minimal volume orthogonal hexahedron whose three orthogonal edges stay within the specified aspect ratio limit. It is the purpose of MBE to find the orientation angle of the minimum volume embedding box in 3-D space, thus determining the angle for slicing the 3-D relaxation pattern into each layer. Basic algorithm of MBE is first explained in section II in its reduced form in 2-D space which can, by itself, be applied to cell-row assignment in the standard placement problems. Extension into the 3-D case is explained in section III with a simple example circuit containing 80 functional blocks.

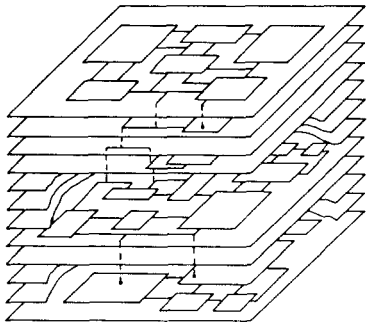


Fig.1. A sketch of 3-dimensional hybrid IC.

II. 2-D Algorithm

For the purpose of illustration, we first describe a 2-D version of MBE algorithm. Fig.2(a) shows the distribution of dots representing the circuit elements in their respective equilibrium positions as a result of the force directed relaxation in 2-dimensional space, where the origin of the x,y coordinates has been shifted to the center of mass (CM) point of the dot pattern. Determining the optimal tilt angle (θ) of the embedding box relative to x-axis, such that the area of the box contains more than a certain major fraction, for example, 90% of the points(in terms of the area of the functional blocks represented by the points), is performed by a procedure, MBE written below (Minimality of the area of

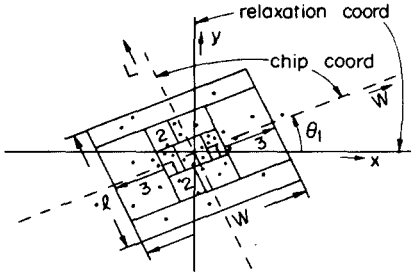


Fig.2. (a) Dot pattern denoting the equilibrium positions of the circuit elements after 2-D force directed relaxation in the relaxation coordinates (x, y) and the chip coordinates (w, l), having origins at the mass center points. (b) trajectory of point in chip coordinates (w, l) representing the growth of embedding lines for aspect ratio constraint and a bounding curve for finding the minimal chip area are also shown.

the embedding box in the relaxation space is assumed to imply a closest match between the pattern in relaxation space and the final layout pattern in chip space);

```
procedure MBE_2D;
bound_area = big_value;      1* bounding function
                               in branch and
                               bound */
for θ = O to π/2 by δ1 do  /* scan orientation
                               angles between 0
                               and π/2 */
   cur_w = small_value;    /* Current width and
                               Current length of
                               the */
   cur_1 = small_value;    /* rectangle is in-
                               itially assigned
                               small values */
   cur_dim = cur_w;        /* first expanding
                               direction in
                               'width' direc-
                               tion */
   while (cur_w* cur_1) <= bound area do /*
                               compare with the
                               area of smallest
                               embedding recta-
                               gle caluculated
                               earlier */
    increase cur_dim by π/2;
    if (samples included in box) >= 90%
                           /* ends if > = 90%
                              of the blocks are
                              included */
    bound_area =  cur_w * cur_1 ; /* set area
                              recorded */
    best_angle = θ;        /* set best angle
                              obtained so far */
    break;
   endif;
   if (increasing rate <= some_valuel) or
                           /* lowest new mem-
                              ber rate */
     max (cur_w/cur_1,cur_1/cur_w)> = some_
     value 2 /* upper limit of the aspect ratio */
     swap cur_dim;         /* alternate expand-
                              ing direction of
                              the embedding
                              box if conditions
                              are met */
    endif;
   endwhile;
  endfor;
end. /* MBE_2D */
```

Two different coordinate systems are shown in Fig.2 (a). One (shown in solid lines) is the relaxation coordinate system (x,y) in which the dot pattern was obtained through the force-directed relaxation, while the other axes (dotted lines) represent the directions for box expansion, and is called the chip coordinate (W,L-coordinate). For a certain value of θ, we keep a record of the width (w) and length (l) of the embedding box in the wl-space shown in Fig.2 (b). A point, P(w_1, l_1) in wl-space (Fig.2(b)) corresponds to a rectangle in the xy-space (Fig.2(a)) centered at the origin and has the edge lengths, w_1 and l_1, respectively. The growing direction of the box in xy-space is

alternated between two orthogonal directions (L - and W-axis) if either of the following conditions is met;

i) the number of points newly included into the box per unit length elongation of the box is less than some value, or
ii) aspect ratio limit is reached.

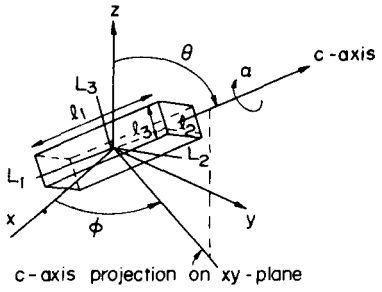
The path in Fig.2(b) composed of (w,l)-value pairs represent the growth history of the embedding box for a certain tilt angle value (θ_1). There are three bounding curves in Fig.2(b). Two are from the aspect ratio limit of the embedding box, while the third one, wl = const, is a bounding function for the subsequent trials with other values for θ, denoting the area of the minimum area embedding box obtained so far.

III. 3-D Algorithm

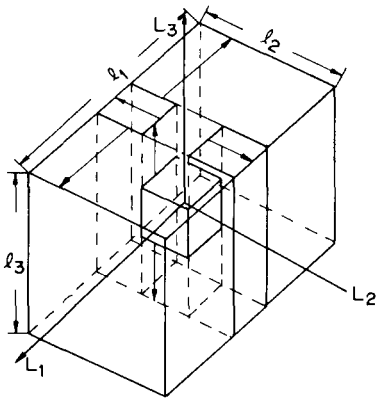
MBE algorithm was explained in the preceeding section for 2-D case, while its major application is in 3-D case. We can easily extend the 2-D algorithm into its 3-D version with some modifications such as

i) Force-directed relaxation is performed in 3-D space.
ii) The rectangular box in 2-D becomes the orthogonal hexahedron in 3-D.
iii) The aspect ratio range limit is applicable for any pairs among three edge lengths of orthogonal hexahedron.

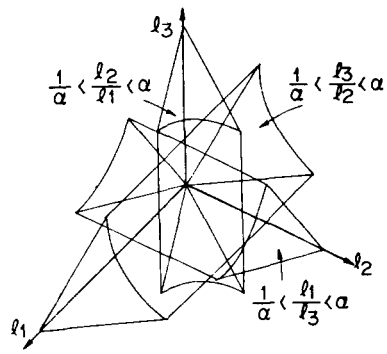
Fig.3(a) shows the xyz-space where 3-D dot pattern exists. We have three different angle values, θ, ϕ and α, to uniquely represent the orientation of the orthogonal hexahedron centered at the origin. Here, cube axis (c-axis) denotes the surface normal vector (centered at the origin) whose arrowhead resides within (+x, +y,+z) octant. In Fig.3(a), θ denotes the angle between z-axis and c-axis, ϕ denotes the angle between x-axis and the c-axis projected on the xy-plane, while α denotes the rotation angle around c-axis. The ranges of angles to be covered for θ, ϕ and α, are $(0, \pi/2)$ for all cases. Fig.3(b) shows the growth of 3-D box in 3 orthogonal directions in L_1, L_2, L_3,-space, while (c) shows the 3 sets of bounding facets, each of which represent $\frac{1}{\alpha} < \frac{l_j}{l_i} < \alpha$, $l_i \times l_j \times l_k < b$,



(a)



(b)



(c)

Fig.3 (a) Orientation of the embedding orthogonal hexahedron as represented by (θ, ϕ, α) in the 3-D relaxation space (x,y,z)
(b) Expansion of the embedding orthogonal hexahedron in L_1, L_2 and L_3-axis direction alternatingly
(c) 3 sets of bounding facet as given the aspect ratio constraint $(\frac{1}{\alpha} < \frac{l_j}{l_i} < \alpha)$, and bounding value which is the minimum volume obtained so far $l_i \times l_j \times l_k < b$ for $i, j, k \in 1, 2, 3$

where $i,j,k \in 1, 2, 3$, and b denotes the value of the current bounding function. After the orientation of the minimum volume embedding box is obtained, we choose the slicing plane as parallel to one of the three facet planes. Fig.4 shows the 3-D dot relaxation pattern and an illustration of the layering process using a set of slicing planes. The number of dots, or more specifically, the sum of the area of functional blocks represented by each dot, are evenly distributed among the slices into which the whole volume is divided by a set of parallel slicing planes.

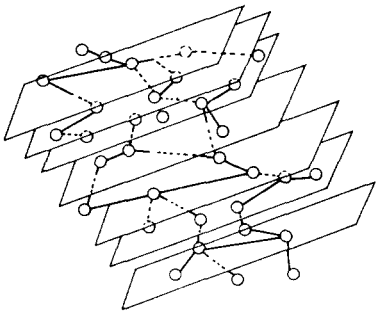


Fig.4. Equilibrium positions of the functional blocks interconnected by nets, and the layer assignment by a set of parallel slicing planes.

IV. Discussions and Concluding Remarks

We implemented the 3-D MBE algorithm in a C program. A circuit consisting of 80 functional blocks and 100 interconnecting nets was used as an example. The result of layer assignment into 4 layers using 3-D MBE procedure was postprocessed by a 2-D placement within each layer using 2-D force-directed relaxation and 2-D packing using the block rotation and the zone refining concept [6]. The dot pattern and the final placement result for each layer are shown in Fig.5(a) through(h). The CPU time consumed was 5 min on VAX 11/780. We are presently working on a more efficient angle sampling scheme, since the fluctuation of the area (volume) of the embedding box according to the samm tilt angle change would be generally small.

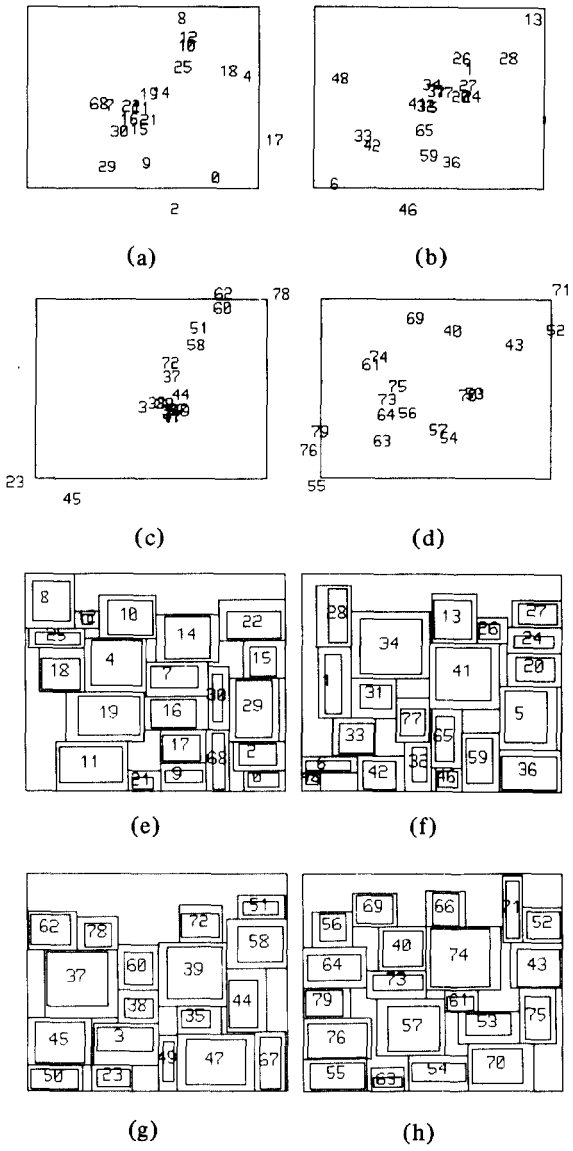


Fig.5. Test run example: a circuit consisting of 80 functional blocks and 100 inter-block nets was placed in 4 layers, according to the layer assignment thru MBE procedure, 2-D force-directed relaxation in each layer with the constraints posed by the placement configuration in the neighbor layer, and block packing using rotation and zone refining. (a), (b), (c), (d): 2-D relaxation pattern in the layer 1,2,3, and 4
(e), (f), (g), (d) : Final Block layout result on the layer 1,2,3 and 4

References

[1] M.A. Breuer ed., *Design Automation of Digital Systems, Vol. 1, Theory and Techniques,* Prentice-Hall, 1972.

[2] N.P. Chen, C.P. Hsu and E.S. Kuh, "The BBL layout System for VLSI design", Proc. *Int'l conf. on VLSI, Elsevier Science Publishers,* North-Holland, 1983.

[3] K. Maling, S.H. Mueller and W.R. Heller, "On Finding Optimal Rectangular Package Plans", *Proc. of 19th Design Automation Conference,* pp. 663-670. 1982.

[4] N.R. Quinn and M.A. Breuer, "A Forced-Directed Component Placement Procedure for PCB's," *IEEE Trans. on Circuits and Systems,* vol. CAS-26, no. 16, pp. 377-388. June 1979.

[5] B.T. Preas and W.M. Van Cleemput, "Placement Algorithms for Arbitrarily Shaped Blocks", *Proc. of 16th Design Automation Conference,* pp. 474-480, 1979.

[6] H. Shin, A.L. Sangiovanni-Vincentelli and C.H. Sequin, "Two-dimensional Compaction by Zone Refining", *Proc. 23rd Design Automation Conference,* pp. 115-122, 1986.