

Constraint Condition of the Loop Filter for the Convergence of Random Jitter Accumulation in Digital Repeater Chain

(디지털 중계단에서 랜덤 지터 누적의 수렴을 위한
루우프 여파기의 제한 조건)

柳 興 均*, 安 秀 桔*

(Heunggyoon Ryu and Souguil ANN)

要 約

디지털 중계기에 사용되는 2차 PLL (phase-locked loop) 회로의 랜덤 지터 누적을 수렴시키기 위한 루우프 여파기의 제한성을 제시하였고, 50번째 중계단, $BW = 100.0\text{KHz}$, $1.0 \times 10^{-6} \text{ [W/Hz]}$ 의 백색 가우시안 잡음하에서 이 제한성을 확인하였다.

또한 이 제한성을 만족시키면 랜덤 누적 지터와 정렬 지터가 포화 특성을 갖게 됨을 보였다.

Abstract

The constraint condition of the loop filter is presented for the convergence of the random jitter accumulation of the 2-nd order PLL (phase-locked loop) circuit used in digital regenerative repeater. This condition is confirmed under the assumption that the number of repeater chain is 50, bandwidth is 100.0KHz, the power spectral density of white Gaussian noise is $1.0 \times 10^{-6} \text{ [W/Hz]}$.

Also, it is shown that if the condition is satisfied, the accumulated random jitter and the alignment jitter will have the saturation characteristics.

I. Introduction

CCITT defines the jitter as "a short time variation of the significant instants of the digital signal from their ideal pulse position in time domain." In repeater chain, the main source is the timing clock recovery circuit which is generally implemented by PLL scheme. According to the report of T. Shimamura and I. Eguchi [1], the proper value of damping factor is 5 to 8 when the number of

repeater chain is 100, 15 to 18 when it is 1000 in the viewpoint of minimizing the system/random jitter accumulation in case that the active-lag loop filter is used for the PLL timing clock recovery circuit.

But the global transfer function $H(j\omega)$ whose loop filter is active-lag type always has a maximum greater than 1.0 for some nonzero ω . Then the jitter peaking is generated so that both the absolute jitter power and the local sampling angle power diverge exponentially.

In this paper, it is reviewed how the total random timing noise accumulates through the repeater chain and that the constrained 2-nd order PLL whose loop filter is a kind of phase-

*正會員, 서울대학교 電子工學科
(Dept. of Elec. Eng., Seoul Nat'l Univ.)
接受日字: 1986年 8月 14日

lead type has the convergence properties of the random accumulated jitter and alignment jitter.

II. Growth of Random Timing Noise [5]-[7]

Fig. 1 shows that for random noise consideration, self-timed regenerators can be represented by a cascaded sequence of timing filters and additive random noise source which is assumed to be Gaussian and flat within the system bandwidth.

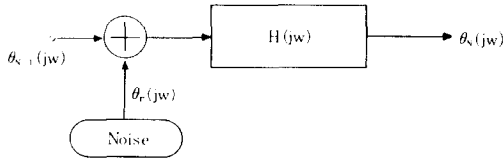


Fig.1. N-th Stage of Repeater Chain.

The input signal to N-th stage is as follows. [6]-[7]

$$f(t) = \sum_n a_n g(t-nT - \theta_{N-1}(t)) \quad (1)$$

where a_n is the binary data, $g(t)$ is the transmitted waveform, T is the period of data symbol, $\theta_{N-1}(t)$ is the variational angle of timing signal whose power spectral density is $|\theta_{N-1}(jw)|^2$.

The random phase noise $\theta_r(t)$ introduced at each regenerator is due to the thermal noise, shot noise, and other data independent effects.

$\theta_r(t)$ has the power spectral density such that the expected value $\langle |\theta_r(jw)|^2 \rangle = S_r$ [W/Hz] which is constant within the bandwidth of timing filter. Since the random noise is uncorrelated at each stage of regenerator, at the last N-th stage the P.S.D of the output random timing noise is expressed in eq. (2).

$$S_{\theta_N} = \sum_{i=1}^N S_r |H(jw)|^{2i} \quad (2)$$

where $H(jw)$ is the closed-loop transfer function of PLL used in timing clock recovery

circuit. Therefore, the total timing noise power is then

$$P_{\theta_N} = \int_{-\infty}^{\infty} S_{\theta_N} df = \sum_{i=1}^N \int_{-\infty}^{\infty} S_r |H(jw)|^{2i} df \quad (3)$$

Under the assumption that the angle variation is small enough for the PLL to be validly represented by its linear model.

$$\theta_N(s) = H(s) [\theta_{N-1}(s) + \theta_r(s)] \quad (4)$$

and the PD (phase detector) output error (i.e. regenerator sampling angle $\phi_N(t)$) is depicted by

$$\phi_N(s) = [1-H(s)] [\theta_{N-1}(s) + \theta_r(s)] = \frac{1-H(s)}{H(s)} \theta_N(s) \quad (5)$$

The phase error spectral density is

$$S_{\phi_N} = S_{\theta_N} |1 - H(jw)|^2 / |H(jw)|^2 \quad (6)$$

and the random phase error power is

$$P_{\phi_N} = \int_{-\infty}^{\infty} S_{\phi_N} df = \sum_{i=1}^N \int_{-\infty}^{\infty} S_r |1 - H(jw)|^2 |H(jw)|^{2i-2} df \quad (7)$$

Since in eqs. (3), (7), S_r is constant within the bandwidth of the loop whose frequency characteristic is similar to the low-pass filter, the closed-loop transfer function $H(jw)$ must be considered in order to investigate the convergence of random timing noise growth as the number of repeater chain increases.

III. Type of Loop Filter

The closed-loop transfer function $H(s)$ used in timing clock recovery circuit (i.e. timing filter) is well-represented as follows [3]-[5].

$$H(s) = \frac{K \cdot F(s)}{s + K \cdot F(s)} \quad (8)$$

where $F(s)$ is the loop filter in PLL,
 $K = K_p \cdot K_v$,
 K_p is the transfer gain of phase detector,
 K_v is the transfer gain of voltage controlled oscillator (VCO).

At first, in case $F(s) = 1.0$, i.e. the 1-st order PLL, $H(j\omega)$ has no jitter peaking so that $|H(j\omega)| < |H(0)| = 1$ for any other frequency. And more importantly, the sampling error $\theta(t)$ in each regenerator in eq. (7) would be always less than some limit which is independent of N (number of repeater chain). This phenomenon is very similar to that of a sequence of RLC passive resonant circuits [2] [5] [6] [7].

But the 1-st order PLL does not have the better performance than the 2-nd order PLL whose loop filter is active lead-lag type because of the wide noise bandwidth, less SNR processing gain and even poorer acquisition characteristics.

Usually, well-acceptable loop filter with $F(s) = 1 + a/s$ can be used but in this case $H(s) = K \cdot F(s)/(s + K \cdot F(s))$ has jitter peaking, namely the absolute value of $H(j\omega)$ always has a maximum greater than 1.0 for some nonzero frequency, which can be easily proved.

As seen in eq. (3), the peaking will be accumulated exponentially for a large number of repeater chain. This result is also observed for the 3-rd order PLL timing filter.

Here, the more general active 1-st order loop filter is shown in Fig. 2.

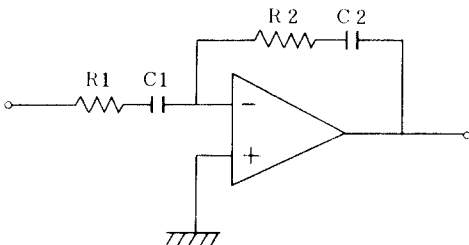


Fig.2. Active 1-st Order Loop Filter.

If $R1 = R2$ and output is inverted, then

$$F(s) = \frac{s + a}{s + e} \quad (9)$$

where $a = 1/(R1 \cdot C2)$
 $e = 1/(R1 \cdot C1)$

Combining eq. (9) into eq. (8), eq. (10) can be obtained.

$$H(s) = \frac{K \cdot S + K \cdot a}{s^2 + (e + K) s + K \cdot a} \quad (10)$$

The constrained condition that in eq. (10) the absolute value of $H(j\omega)$ is always less than 1.0 (i.e. no jitter peaking) for any value of ω is represented as in eq. (11).

$$e^2 + 2 \cdot e \cdot k > 2 \cdot a \cdot k \quad (11)$$

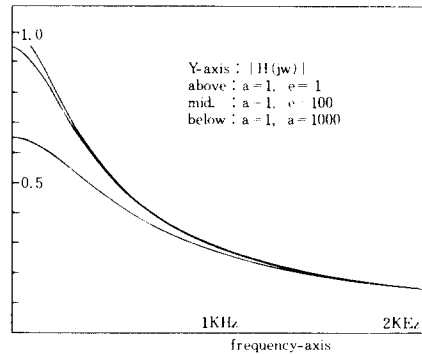


Fig.3. Constrained Transfer Function $H(j\omega)$.

In practical digital/optical communication systems. $K = K_p \times K_v = 0.0593[\text{V/rad}] \times 31400[\text{rad/V}] = 1862.02$ is used for 1344 channel (2 x T3 level) 90Mbps system and the values of a and e are positive.

For the above value of K , the amplitude characteristics of $H(s)$ in eq. (10) satisfying the constrained condition of eq. (11) is shown in Fig.3 as the value of e varies among 1,100 and 1000 for $a=1.0$. The more satisfiable with the condition the lower the curve.

IV. Numerical Results

It is assumed that the accumulated jitter

(total random timing noise power) is calculated for the value observed at the 50-th stage of repeater chain and the noise power spectral density is 1.0×10^{-6} [W/Hz] and the system bandwidth is taken enough as 100.0KHz.

For the fixed value of a, the power of the accumulated jitter and phase error power change with the variation of e as shown in Fig. 4,5,6,7,

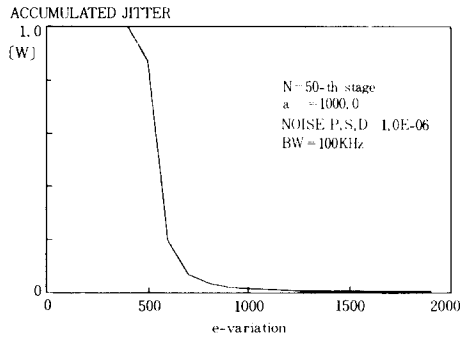


Fig.4. Convergence of Accumulated Jitter (1).

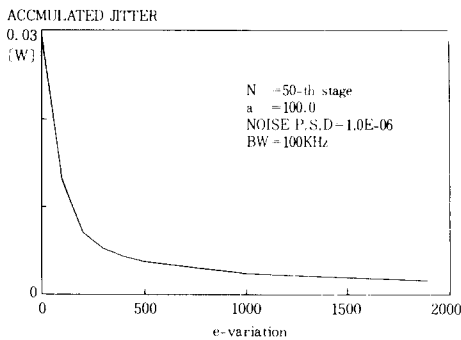


Fig.5. Convergence of Accumulated Jitter (2).

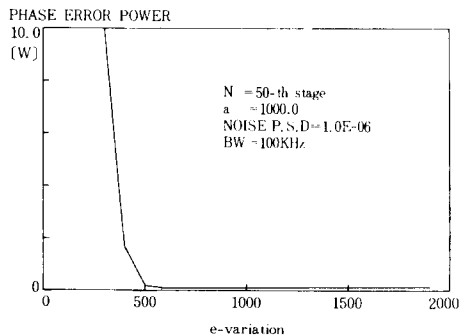


Fig.6. Convergence of Phase Error Power (1).

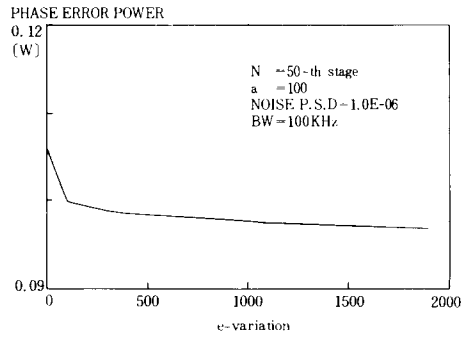


Fig.7. Convergence of Phase Error Power (2).

In Fig. 4 and Fig. 6 the value of e must be taken at least 1000,0 for the value of a=1000,0 in order for the accumulated jitter and the phase error (sampling error) power in each regenerator to be minimized to the satisfaction of CCITT which recommend the constrained value of -2 dB (0.63) of the accumulated jitter in the last receiver. And Fig.5 and Fig. 7 show that the properly small value of e about at least 100.0 will be acceptable for the value of a=100.0

Next, Fig.8,9, 10 show that the accumulated jitters and alignment jitters have the different magnitudes for the different values of a and e as the number of repeater chain grows.

In Fig.8. we can see that the total random timing noise exponentially accumulates because the loop filter coefficients don't satisfy the constrained condition of $|H(j\omega)| < 1.0$. Since the satisfaction for the constraint is richer in Fig. 10 than in Fig. 9, the convergence property is more obvious and earlier in

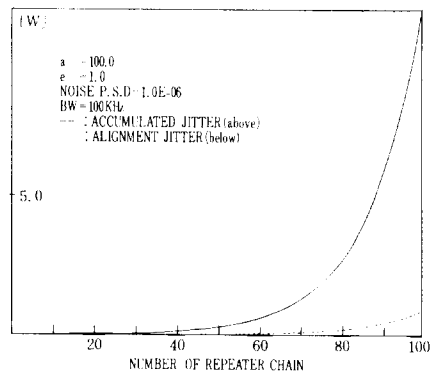


Fig. 8. Accumulated/Alignment Jitters (1).

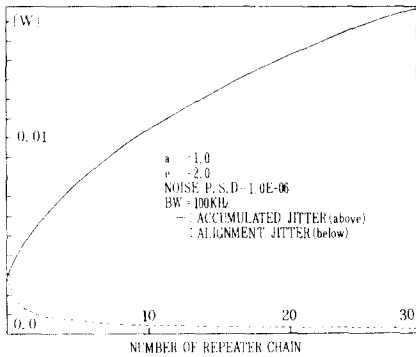


Fig.9. Accumulated/Alignment Jitters (2).

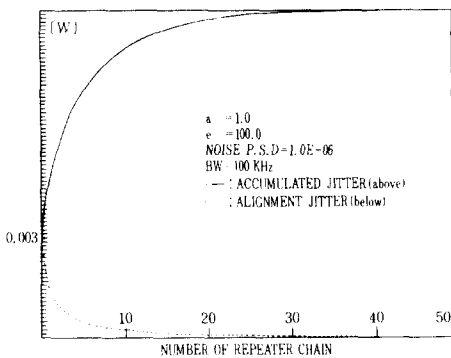


Fig.10. Accumulated/Alignment Jitters (3).

Fig. 10 than Fig. 9. More importantly, the more satisfiable with the condition the smaller the accumulated jitter.

V. Conclusion

We have derived the constraint condition for the 2-nd order PLL circuit which is used for the timing clock recovery in digital data regenerative repeater. For the conviction of the condition we have confirmed the convergence of the accumulated jitter and phase

error output power with the variation of the condition through the computer simulation as shown in Fig. 4, 5, 6, 7.

And in the case of fully-satisfiable condition, the total random timing jitter does not accumulate more than the limit of -2dB (0.63) recommended by the CCITT. In future, it remains that the well-constrained condition will be found in optical regenerative repeaters which include the optic devices and circuit and interfaces with the digital circuit.

References

- [1] T. Shimamura and I. Eguchi, "An analysis of jitter accumulation in a chain of PLL timing recovery Circuit", *IEEE*, vol. COM-25, no. 9, pp. 1027-1032, Sept. 1977.
- [2] C.J. Byrne, B.J. Karafin and D.B. Robinson, "Systematic jitter in a chain of digital regenerators," *B.S.T.J.* vol. 42, pp. 2679-2714, nov. 1963.
- [3] K. Feher, *Digital communication*, Prentice-Hall, 1983.
- [4] F.M. Gardner, *Phaselock Techniques*, Wiley, 1979.
- [5] J.T. Harvey and J.W. Rice, "Random timing noise growth in a cascaded digital regenerator chain," *IEEE Trans. on Comm.* pp. 969-971, Aug. 1973.
- [6] O.E. De Lange, "The timing of high-speed regenerative repeater." *B.S.T.J.*, vol. 37, pp. 1455-1486, Nov. 1958.
- [7] S. Pupolin and C. Tomasi, "Spectral analysis of line regenerator time jitter," *IEEE, Trans. on Comm.* vol. 32, no. 5, pp. 561-566, May 1984.