Fabrication of Polysilicon Resistors Compensated with Boron and Phosphorous Ion-Implantation

(Boron과 Phosphorous 이온주입에 의한 다결정 실리콘 저항의 제조)

金 知 範*, 崔 民 成*

(Ji Bum Kim and Min Sung Choi)

要 約

본 실험에서는 높은 면저항(Rs 1K-33KΩ/□)을 갖는 다결정 실리콘 저항을 boron과 phosphorous 이온주입을 이용해서 제작하였다. 기존의 boron 이온주입에 의한 다결정 실리콘과 비교해서, boron과 phosphorous 이온주입에 의한 다결정 실리콘 저항의 경우 도핑농도에 따른 면저항값의 변화가 한 지수가 낮으며, 같은 면저항값에 대해서는 같은 다결정 실리콘 저항의 온도계수(TCR) 값을 얻을 수 있었다. 또한 grain boundary trapping 이론을 이용해서, boron과 phosphorous 이온주입에 의한 다결정 실리콘 저항의 정성적인 전기적 전도기구(electrical conduction mechanism)를 설명하였다.

Abstract

High value sheet resistance (R_S' 1K - 33KΩ/□) polysilicon resistors were fabricated using double ion implantation with boron as the major dopant and phosphorus compensation. It is observed that R_S sensitivity to the net doping concentration is decreased by one order of magnitude compared to the conventional (boron implanted) polysilicon resistors. The temperature co-efficient of resistance (TCR) measured between 25°C and 125°C shows equivalent values to those of non-compensated resistors for the same R_S. A qualitative electrical conduction mechanism for compensated polysilicon resistor is proposed, based on the existing grain boundary charge trapping theory.

I. Introduction

The electrical properties of implanted polysilicon resistors were discussed by previous investigators (1-4). This paper reports the effect of boron-phosphorus double-ion implantation on the electrical characteristics of polysilicon resistors. There has been a report (5) on the calculation of TCR (temperature coefficient of resistance) for the compensated (boron-phosphorus doped) single crystal silicon resistors, which predicted lower TCR than the uncompensated resistor. However, no data is available in the literature on the performance of any compensated polysilicon resistor. The objective of this study was to find the effect of electron-hole compensation on the electrical properties of polysilicon resistors. The observed characteristics of the compensated polysilicon resistors demonstrated a big improvement in the control of high value

*正會員, 金星半導體株式會社 研究所
(GoldStar Semiconductor Ltd., R & D)
接受日字 : 1987年 4月 20日

sheet resistance (1K - 33K Ω/□) polysilicon resistors.

II. Experimental Procedures

The experimental procedure is basically the same as explained in Ref. 4 except for some details: 3000 or 4000Å of low pressure chemical vapor deposition (LPCVD) polysilicon was deposited at 625°C using silane on the top of thermal oxide (3700Å) grown on p-type substrates.

After 2000Å of thermal oxide was formed on top of the polysilicon, a boron-phosphorus double-ion implantation was done to produce a net doping concentration of p-type. Various background doping concentrations were first achieved by boron-ion implantation and then different doses of phosphorus were implanted immediately after the boron. Annealing was done at 1000°C for 81 minutes (3000Å thick film) or at 950°C for 64 minutes (4000Å thick film). The resistor was defined using photolithography and RIE of the cap oxide and polysilicon. CVD nitride was deposited before contact was made to the resistors. Then the contact area was defined. Platinum silicide (PtSi) was formed as a diffusion barrier metallurgy before the contact metal is deposited. Electron-gun evaporated platinum or sputtered platinum was used to form the silicide. Aluminum-copper alloy was deposited by e-gun-evaporated deposition for the contact metallurgy. Annealing was done at 400°C for 1-2 hours after the Al metal was deposited. Sheet resistance (R_S) was measured for 24 different sites per wafer at 25°C and 125°C using standard 4 point probe structure. The measurement was done at different steps (before Pt deposition, after PtSi formation and after Al/Cu deposition).

III. Experimental Results

1. Sheet Resistance (R_S) vs. Doping Concentration Characteristics

Table 1 contains summary data for the experiment. In this table, N_A represents background boron concentration and N_A-N_D gives the excess boron concentration after compensation was done with phosphorus doping. R_S [11] and R_S [12] with their standard deviation (σ) represent the R_S values measured at 25°C before and after PtSi was formed respectively. Temperature coefficient of resistance (TCR) between 25°C and 125°C is also shown in percent from the R_S values measured at the Si level (before PtSi was formed). Half of the wafers had the PtSi formed by sputtered Pt deposition and the other half by e-gun evaporation as indicated in the table.

Figure 1 shows the plot between log R_S vs. the excess boron doping concentration (N_A-N_D) from data in Table 1 (Job #0415, 0712). It also contains data from Ref. 4 for the samples that received single ion implantation with boron. For all the samples in this figure, the process conditions were identical for both uncompensated and compensated sample pairs except for ion implantation. Fig. 1 demonstrates the striking effect of compensation on the sensitivity of R_S to the doping concentration. For example, R_S changes by approximately two orders of magnitude as the doping concentration changes by one order of magnitude for the uncompensated resistor. However, the R_S change is less than one order of magnitude for the compensated resistors for the same amount of change in doping concentration. This phenomenon was repeated by another run (job 2736) which purposely had a split of different background doping concentration varying from $7.3 \times 10^{18}/cm^3$ to $2 \times 10^{19}/cm^3$. The results of this run and job 0712 from Fig. 1 are plotted in Fig. 2. It is seen that 1K Ω/□ -33KΩ/□ of R_S was achieved with different background doping concentrations.

By choosing different background doping concentrations there can be several ways of obtaining the same R_S. As an example, 20K Ω/□ of R_S was obtained at both effective doping concentrations of $2.4 \times 10^{18}/cm^3$ and $4.2 \times 10^{18}/cm^3$ depending on the background concentration of $9.1 \times 10^{18}/cm^3$ and $7.3 \times 10^{18}/cm^3$, respectively (see Fig. 2). This new R_S vs. doping concentration characteristics of compensated polysilicon resistors provide the possibility of tight control of high value R_S.

표 1. Compensation과 면저항값의 관계
Table 1. Effect of Compensation on Sheet Resistance.

JOB #	N_A	$N_A - N_D$	$R_S^{11} \pm \sigma$ (KΩ/□)	$R_S^{12} \pm \sigma$ (KΩ/□)	$TCR^{25-125℃}$ (%)	POLYSILICON THICKNESS (A°) AND ANNEAL CONDITION
2736	2×10^{19}	2×10^{19}	1.67 ± 0.01	1.66 ± .006	−13.0	
2736		10^{19}	3.07 ± 0.059	3.05 ± 0.060	−18.9	
0415		2×10^{19}	1.82 ± 0.017	1.85 ± 0.022	−12.4	
0415		10^{19}	3.10 ± 0.05	3.19 ± 0.05	−17.2	
2736*		9.1×10^{18}	3.53 ± 0.032	3.54 ± 0.03	−19.3	
2736		5×10^{18}	4.56 ± 0.078	4.49 ± 0.069	−23.2	
0415		5×10^{18}	4.44 + 0.10	4.60 ± 0.092	−20.5	3000A°
2736*		1.8×10^{18}	7.50 ± 0.147	7.50 ± 0.119	−28.0	
2736*		0	9.51 ± 0.228	9.44 ± 0.164	−31.2	1000℃
2736*	9.1×10^{18}	9.1×10^{18}	7.18 ± 0.198	7.09 ± 0.094	−27.9	81min
2736*		7×10^{18}	9.33 ± 0.108	9.23 ± 0.096	−32.6	
2736*		3.2×10^{18}	17.15 ± 0.397	16.67 ± 0.339	−39.4	
2736		1.8×10^{18}	18.79 ± 0.108	16.61 ± 0.066	−41.2	
2736*	7.3×10^{18}	7.3×10^{18}	12.16 ± 0.176	11.88 ± 0.097	−34.0	
2736*		5×10^{18}	17.51 ± 0.402	16.67 ± 0.364	−40.8	
2736		5×10^{18}	17.61 ± 0.253	15.25 ± 0.166	−42.2	
2736*		4×10^{18}	21.38 ± 0.219	20.14 ± 0.487	−43.9	
2736*		1.8×10^{18}	33.7 ± 0.992	32.55 ± 0.488	−47.7	
0712	5×10^{19}	5×10^{19}	0.337 ± 0.004	0.340 ± 0.007	+ 8.6	4000A°
0712		1×10^{19}	1.22 ± 0.026	1.28 ± 0.032	− 8.8	950℃
0712		5×10^{18}	1.58 ± 0.056	1.60 ± 0.064	− 9.8	64min.

R^{11} : 25℃, Si
R^{12} : 25℃ PtSi
* : Sputterred Platinum

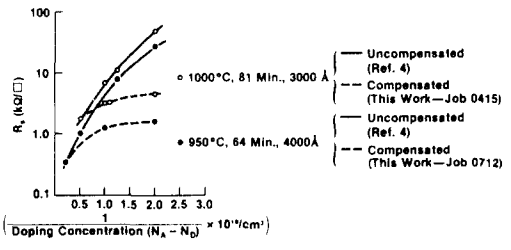

Fig. 1. Effect of Doping and Annealing Temperature on Sheet Resistance (R_S) of Compensated Polysilicon Resistor.

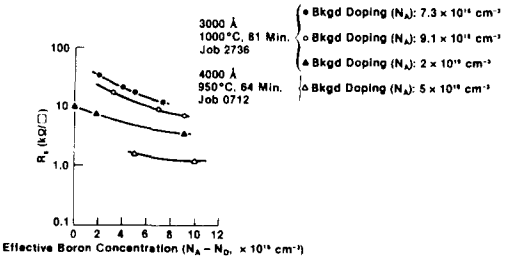

Fig. 2. Effect of Compensation on Sheet Resistance (R_S)

Actually, preliminary data indicate that excellent reproducibility in R_S can be achieved.

In Table 1, it is shown that run-to-run (two jobs) reproducibility of 3.1KΩ/□ and 4.5KΩ/□ was within 0.5% and 1.5% respectively.

2. Temperature Coefficient of Resistance (TCR) for Compensated Polysilicon Resistors.

In the previous report (4), the author showed that the TCR of a boron-implanted polysilicon resistor is only a function of sheet resistance, independent of process variables (ion implantation dose, resistor anneal temperature and time) except for the film thickness. This phenomenon is explained by the grain boundary trapping mechanism of carriers as reported in the literature (1-3).

Figure 3 shows the plot of R_s vs. TCR (%) of compensated polysilicon resistors measured between 25-125°C. For comparison, TCR for the uncompensated polysilicon resistors from Ref. 4 is also included in this figure. It is seen that the data falls on the same curve for both compensated and uncompensated samples. This indicates that the basic electrical conduction mechanism of polysilicon resistor had not changed by double ion implantation. However, for the same effective doping concentration, the compensated resistor has much lower TCR (in magitude) than the uncompensated resistor.

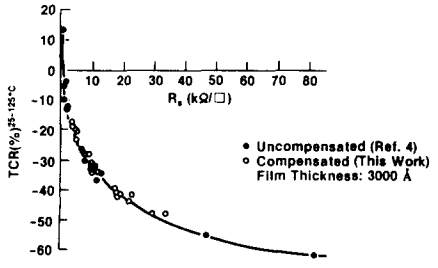

Fig. 3. Temperature Coefficient of Polysilicon Resistors (TCR).

IV. Conduction Mechanism of Compensated Polysilicon Resistors

Polysilicon is a polycrystalline material and is therefore composed of crystallites of different sizes. Each crystallite has a certain crystallographic orientation and is joined to its neighbors through grain boundaries (disordered atomic layers of approximately 1 nm thickness). The electrical conduction mechanism and the band structure of the polycrystalline semiconductor are modified by the grain boundaries. The most widely accepted conduction mechanism is the carrier trapping model described in the previous literature (1-3): The grain boundaries contain carrier trapping sites located at an energy E_T with respect to the intrinsic Fermi level of the crystallites. The density of the trapping sites is measured as a surface charge Q_t/cm^2. The band structure of single crystal silicon can be applied to the polysilicon except in the vicinity of the grain boundaries.

When the polysilicon is doped with N-or P-type materials, the neutral traps become charged by trapping the carriers and thus depleting the crystallites near the grain boundaries. As a result, a potential barrier V_B is built up near the grain boundaries due to the charged traps. The depletion layer width is changed by the amount of charged traps. Consequently the effective carrier concentration and the conductivity of the polysilicon are significantly reduced by the grain boundary effects. The electrical conduction mechanism is assumed to arise mainly from the thermionic emission of effective carriers over the grain boundary potential. The mobility minimum of carriers and the steep slope of the sheet resistance (R_S) as a function of doping concentration is due to the existence of this potential barrier. The greatest sensitivity of R_S to ion implantation dose occurs at intermediate doping levels because at these concentrations, the grain boundary trapping sites are not yet saturated and the potential barrier height is still increasing. At even higher doping levels, the grain boundaries are saturated and both the depletion layer width and the potential barrier height are reduced, resulting in decrease in sensitivity of R_S to dose.

We think the basic mechanism of conduction remains the same for compensated polysilicon resistors as for the uncompensated resistors. However, it is proposed to compensate the doping in the polysilicon, that is, to provide both N-type dopants and P-type dopants, with the effective doping concentration being the difference between the two doping levels. As a result, the grain boundary traps are charged with both kinds of carriers, electrons and holes. The relative

amount of trapped charges between electrons and holes and its associated trapping energy levels are not known. However, if both kinds of carriers are trapped at the grain boundaries, the effective barrier height at the grain boundary would be lowered by the compensated doping even though the net effect of doping is determined by how much one doping concentration exceeds the other. Since electrical conduction is very sensitive to the grain boundary potential height, a slight decrease in potential can greatly modify the sensitivity of the sheet resistance to the effective doping concentration. As stated before, Fig. 3 supports the proposed conduction mechanism for the compensated resistors.

In Table 1, it is noted that R_S is not very high even if N_A-N_D is zero. It is probably because of the physical segregation of phosphorus atoms at the grain boundaries as well as carrier trapping. It is reported that significant amounts of phosphorus atoms can be segregated to the grain boundaries of polysilicon reducing the effective number of dopant atoms (6).

V. Conclusions

High value sheet resistance (R_S, 1 K-33 KΩ/□) polysilicon resistors were fabricated using double ion implantation with boron and phosphorus. The observed R_S sensitivity to the effective doping concentration was significantly reduced compared to the conventional (boron implanted) polysilicon resistors. These characteristics can be utilized for tight control of R_S for the resistors used in integrated circuits. The temperature coefficient of resistance (TCR) measured between 25°C and 125°C showed equivalent values to those of boron implanted polysilicon resistors for the same R_S values. A basic electrical conduction mechanism of compensated polysilicon resistor is proposed based on the existing grain boundary charge trapping theory.

References

[1] J.Y.W. Seto, "The electrical properties of polycrystalline silicon films" *J. Appl. Phys.*, vol. 46, p. 5427, Dec. 1975.

[2] N.C-C. Lu, L. Gerzerg, C-Y, Lu. J.D. Meindl, "Modeling and optimization of monolithic polycrystalline silicon resistors" *IEEE Trans. Electron Devices*, vol. ED-28, no. 7, p. 818, July 1981.

[3] M.M. Mandurah, K.C. Saraswat, T.I. Kamins, "A model for conduction in polycrystalline silicon-part 1: theory" *IEEE Trans. Electron Device*, vol. ED-28, no. 10, p. 1163, Oct. 1981.

[4] 朴鍾泰, 崔民成, 李文基, 金鳳烈, "다결정 실리콘 저항의 전기적 특성," 電子工學會誌, 第23卷, 第6號, pp. 795-800, 11月, 1986年.

[5] P. Norton and J. Brandt, *Solid State Electronics* vol. 21, p. 969, 1978.

[6] M.M. Mandurah, K.C. Saraswat, C.R. Helsm, T.I. Kamins, "Dopant segregation in polycrystalline silicon" *J. Appl. Phys.*, vol. 51, p. 5755, Nov. 1980.