IIR LDM디지탈필터의 구현

Realization of IIR LDM Digital Filters

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요 약

본 논문에서 선형 델타 변조방식을 간단한 아날로그/디지탈 변환기로 이용하여 무한 응답 디지탈 여파기를 구현하는 방법을 제시하였다. 이 방법은 하드웨어 승산기나 펄스 부호변환 아날로그/디지탈 변환기를 필요로 하지 않으므로 종래의 무한응답 디지탈 여파기의 구현방법보다 매우 간단하다. Lee와 Un의 유한응답LDMDF에 비해서 이 무한응답LDMDF는 매우 적은 계산시간이 요구된다.

ABSTRACT

In this paper, we present a method of realizing an infinite impulse response (IIR) digital filter (DF) using linear delta modulation (LDM) as a simple analog/digital (A/D) converter. This method makes the realization of IIR digital filters much simpler than that of conventional ones because it does not require hardware multipliers and a pulse code modulation (PCM) A/D converter. Compared to the finite impulse respponse (FIR) LDMDF of Lee and Un [1], this IIR LDMDF requires significantly less computation time.

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I. INTRODUCTION

Digital filters are normally implemented using pulse code modulation (PCM) for analog-to-digital (A/D) conversion of the input signal. This conventional PCM filter, realized by using multipliers and adders to carry out convolution, is relatively expensive and requires a large number of computations. To avoid these problems, several researchers have studied a new type of digital filters using delta modulation (DM) for A/D conversion of the input signal [1]-[7]. Since the input signal is digitized by a 1-bit word format, this type of filter does not require a hardware multiplier. So far, these studies have been done mostly on finite impulse response (FIR) DM digital filters.

The purpose of this paper is to present a method to realize infinite impulse response (IIR) digital filters using DM as a simple A/D converter for digitization of the input signal.

In what follows, we first present a method to realize IIR LDMDF's, and then compare its performance to that of the equivalent FIR LDMDF with respect to computation time.

II. REALIZATION OF IIR LDMDF

In this section we first consider the realization of a second-order IIR LDMDF, and then discuss the realization of higher-order filters.

Let x(kn) and y(kn) be the filter input and the desired output samples taken at the Nyquist rate. The input-output relationship of a conventional second order IIR digital filter is represented by

$$y(kn) = a_0x(kn) + a_1x(k(n-1)) + a_2x(k(n-2)) - b_1y(k(n-1)) - b_2y(k(n-2)) \tag{1}$$

where a's and b's are coefficients characterizing the filter. Normally, the sampling frequency of DM must be several times higher than the Nyquist frequency. Thus, we consider an IIR LDMDF in which the input sampling frequency by DM is k times the Nyquist rate, but each output sample is produced at the Nyquist rate. If the sampling frequency of DM is sufficiently high, (1) can be approximated by

$$\hat{y}(kn) = \beta\hat{y}(k(n-1)) + X - Y \tag{2}$$

with

$$X = a_0[\hat{x}(kn) - \beta\hat{x}(k(n-1))] + a_1[\hat{x}(k(n-1)) - \beta\hat{x}(k(n-2))] + a_2[\hat{x}(k(n-2)) - \beta\hat{x}(k(n-3))] \tag{3}$$

$$Y = b_1[\hat{y}(k(n-1)) - \beta\hat{y}(k(n-2))] + b_2[\hat{y}(k(n-2)) - \beta\hat{y}(k(n-3))] \tag{4}$$

where $\hat{x}(kn)$ is the predicted input sample by DM, $\hat{y}(kn)$ is its corresponding actual digital output sample, both taken at the Nyquist rate, and β is a scale factor. Eqs.(2),(3) and (4) represent the input-output relationship of an IIR LDMDF.

Fig.1 shows the DM encoder used in an IIR LDMDF. One can see from this figure that the only difference of this encoder from the conventional DM encoder is the analog switch. This analog switch selects the value of β multiplied by the predicted signal at every k-th sampling instant (i.e., at the Nyquist rate); and in other sampling instants, it directly selects the predicted signal. The predicted signal satisfies

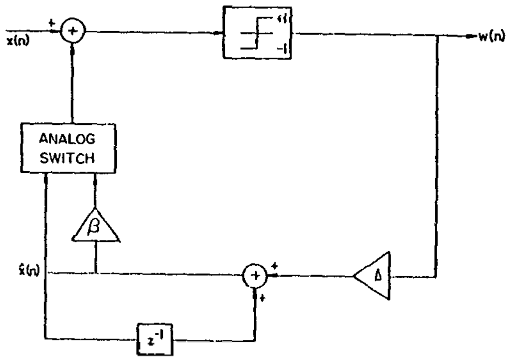

Fig. 1 LDM encoder used in IIR LDMDF.

$$\hat{x}(kn) - \beta\hat{x}(k(n-1)) = \triangle \cdot I(kn) \tag{5}$$

where $\triangle$ is the DM step size, and

$$I(kn) \triangleq w(kn) + w(kn-1) + \cdots + w(k(n-1)+1) \tag{6}$$

w(n) being the comparator output generated at the frequency of K times the Nyquist rate. One can easily see that I(kn) of (6) is an integer, and its absolute value is less than or equal to K. Using (5), we can write (3) as

$$X = a_0\triangle \cdot I(kn) + a_1\triangle \cdot I(k(n-1)) + a_2\triangle \cdot I(k(n-2)) \tag{7}$$

Let us assume that J binary bits including sign bits are used in 2's complement code to represent the integer I(kn), that is,

$$I(kn) = 2^{J-1}[-I(kn)^0 + \sum_{i=1}^{J-1} I(kn)^i \cdot 2^{-i}] \tag{8}$$

where $I(kn)^i$ is the i-th bit of I(kn). Then, substituting (8) in (7), we have

$$X = a_0 \cdot \triangle \cdot 2^{J-1}[-I(kn)^0 + \sum_{i=1}^{J-1} I(kn)^i \cdot 2^{-i}] + a_1 \cdot \triangle \cdot 2^{J-1}[-I(k(n-1))^0 + \sum_{i=1}^{J-1} I(k(n-1))^i \cdot 2^{-i}] + a_2 \cdot \triangle \cdot 2^{J-1}[-I(k(n-2))^0 + \sum_{i=1}^{J-1} I(k(n-2))^i \cdot 2^{-i}] \tag{9}$$

Let us define a function $f_1(\cdot)$ with three binary arguments as

$$f_1(x_0, x_1, x_2) \triangleq [a_0x_0 + a_1x_1 + a_2x_2] \cdot \triangle \cdot 2^{J-1} \tag{10}$$

Then, (9) may be written as

$$X = \sum_{i=1}^{J-1} f_1[I(kn)^i, I(k(n-1))^i, I(k(n-2))^i] 2^{-i} - f_1[I(kn)^0, I(k(n-1))^0, I(k(n-2))^0] \tag{11}$$

where the value of $f_1[I(kn)^i, I(k(n-1))^i, I(k(n-2))^i]$ can be obtained from a read-only memory (ROM) addressed by their arguments since the value of $I(kn)^i$ is 1 or 0.

Let us now define

$$d\hat{y}(kn) \triangleq \hat{y}(kn) - \beta \cdot \hat{y}(k(n-1)) \tag{12}$$

By manipulating in the same way as for X, Y can be written from (4) as

$$Y = \sum_{j=1}^{B-1} f_2[d\hat{y}(k(n-1))^j, d\hat{y}(k(n-2))^j] 2^{-j} - f_2[d\hat{y}(k(n-1))^0, d\hat{y}(k(n-2))^0] \tag{13}$$

where B bits including sign bits are used in 2's complement code, and $f_2(\cdot)$ is defined as

$$f_2(x_1, x_2) \triangleq b_1x_1 + b_2x_2 \tag{14}$$

With (11) and (13), (2) can be written as

$$\begin{aligned}\hat{y}(kn) = {} & \beta \cdot \hat{y}(k(n-1)) + \Big[\sum_{i=1}^{J-1} f_1\{I(kn)^i, \\ & I(k(n-1))^i, I(k(n-2))^i\} \cdot 2^{-i} - f_1\{(I(kn)^0, \\ & I(k(n-1))^0, I(k(n-2))^0\}\Big] \\ & -\Big[\sum_{j=1}^{B-1} f_2\{d\hat{y}(k(n-1))^j, d\hat{y}(k(n-2))^j\} \cdot 2^{-j} \\ & - f_2\{d\hat{y}(k(n-1))^0, d\hat{y}(k(n-2))^0\}\Big]\end{aligned} \tag{15}$$

The functions $f_1(\cdot)$ and $f_2(\cdot)$ can take on only $2^3(=8)$ and $2^2(=4)$ distinct values, respectively, depending on the binary vectors which form the arguments of each function.

We can see from (15) that only J additions and (J-1) shifting operations are required for computation of X, and that B additions and (B-1) shifting operations for Y. Since computations of X and Y are performed concurrently, and B is in general larger than J, the total computation time for each digital output is determined by the time required for the computation of Y.

Also, we can see from (15) that it is desirable to compute $\beta \cdot \hat{y}(k(n-1))$ digitally without multiplication. Note that β, which is a leak factor used in the DM encoder, is less than or equal to 1. Thus, we can make the value of β some fixed value as

$$\beta = 1 - 2^{-m} \tag{16}$$

where m is an integer indicating the number of operations shifting right by one bit. Accordingly,

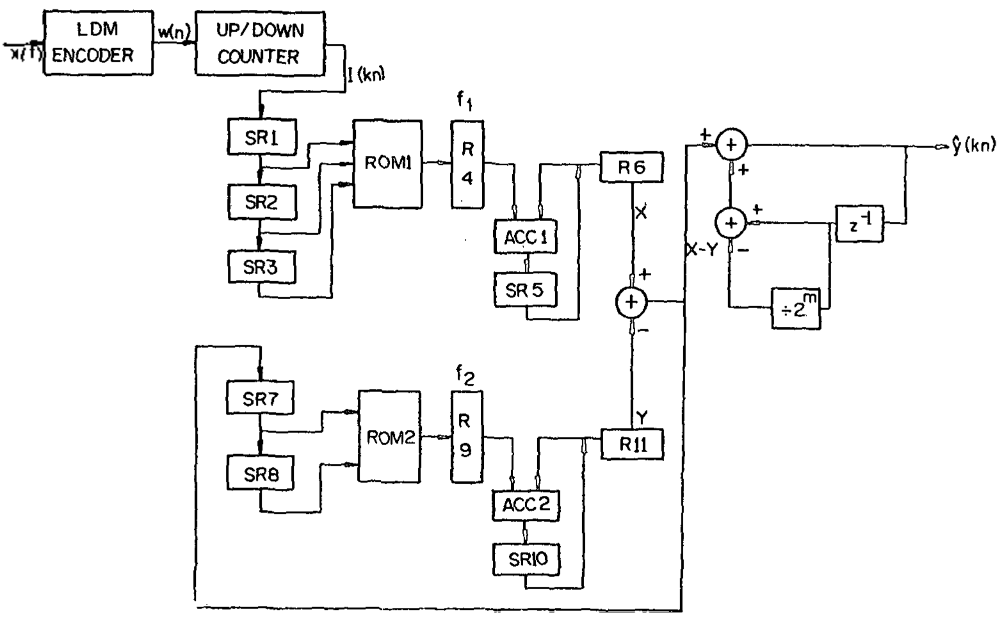

Fig. 2 Realization of a second-order IIR LDMDF.

it is easy to compute $\beta \cdot \hat{y}(k(n-1))$ using a shift register and an adder without a multiplier. Consequently, one can see from (15) that the digital output can be generated with additions and shifting operations only.

A block diagram for the realization of an IIR LDMDF is shown in Fig.2. An analog input signal is digitized bit-by-bit at the frequency of K times the Nyquist rate by an LDM encoder, and an up/down counter accepts the bit stream from the LDM encoder during the interval of Nyquist sampling and counts I(kn). This counter output, I(kn), is loaded into the shift register SR1, and then the up/down counter is cleared. The data in SR1 is shifted to the SR2 and SR3 at each Nyquist sampling time. The data in the shift registers, SR1, SR2, and SR3 are serially moved by one bit at each shift with the least significant bit first. At each shift, a new vector $\{I(kn)^i, I(k(n-1))^i, I(k(n-2))^i\}$ appears at the input of ROM1, and the output f_i is loaded into the register R4. After J additions and (J-1) right-shifting operations by the accumulator ACC1 and the shift register SR5, a final value of X in (15) (which is rounded to B bits0 is stored in the register R6. In the same way as above, computation of the third term Y in (15) is performed concurrently with that of the second term X. The difference (X-Y) is then loaded into the shift register SR7, and it is used to compute the next output sample $\hat{y}(k(n+1))$

An IIR LDMDF with its order higher than 2 can easily be realized with the increase of the memory to store the intermediate outcomes for direct-form realization. Also, the higher-order IIR LDMDF can be realized by having several second-order or first-order IIR LDMDF's in parallel.

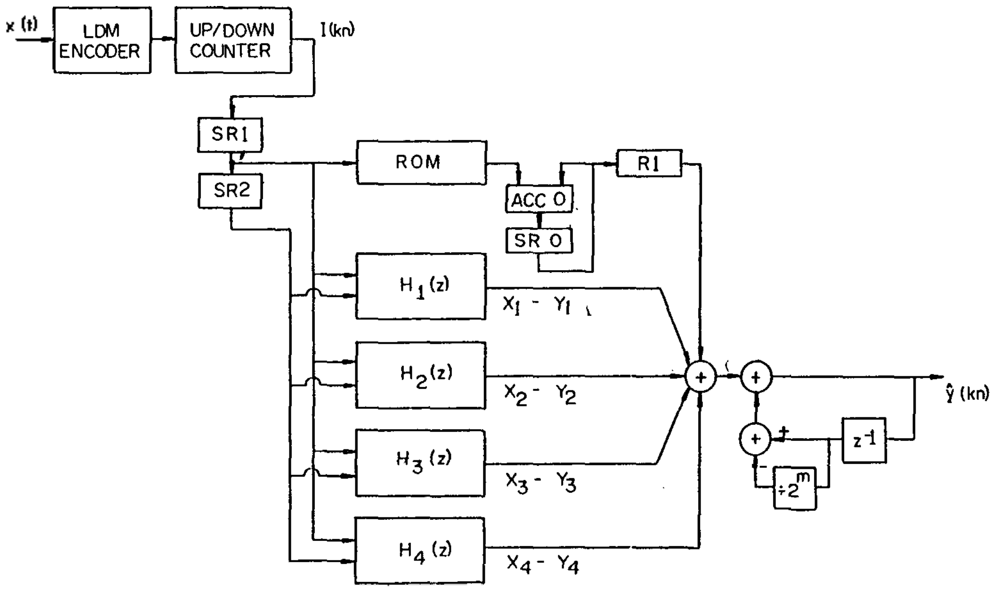

Fig. 3 Parallel realization of an 8-th order IIR LDMDF using 4 second-order sections.

An N-th order IIR digital filter may be expressed as

$$H(z) = C + \sum_{i=1}^{P} H_i(z) \tag{17}$$

where C is a constant, $H_i(Z)$ is either a second-order or a first-order section. In Fig.3 a parallel realization of an eighth-order IIR LDMDF is shown. In the same way as for the second-order IIR LDMDF, $\triangle \cdot C \cdot I(kn)$ $(=C\{\hat{x}(kn)-\beta\hat{x}(k(n-1))\})$ is obtained by the accumulator ACCO and the shift register SRO after repeated J additions and (J-1) shifting operations.

III. SIMULATION RESULTS AND DISCUSSION

Simulations have been done for the fourth-order IIR LDMDF, and a comparison has been made between this IIR LDMDF and its equivalent FIR LDMDF with respect to computation time. In our simulation, the input signal was a flat Gaussian signal which was obtained by passing Gaussian random samples through a

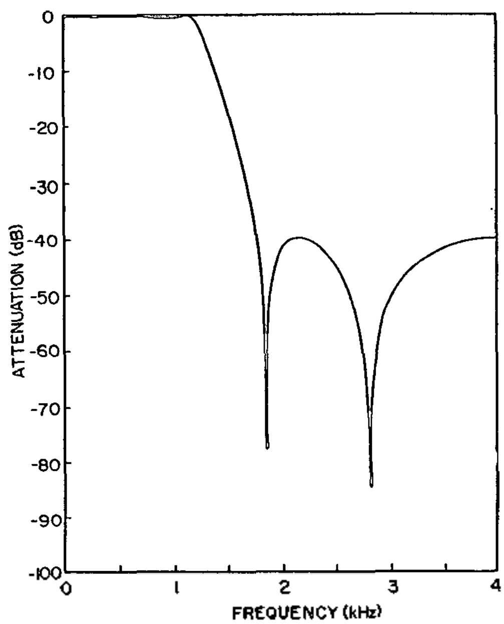

Fig. 4 Magnitude response of fourth-order IIR LDM low-pass digital filter.

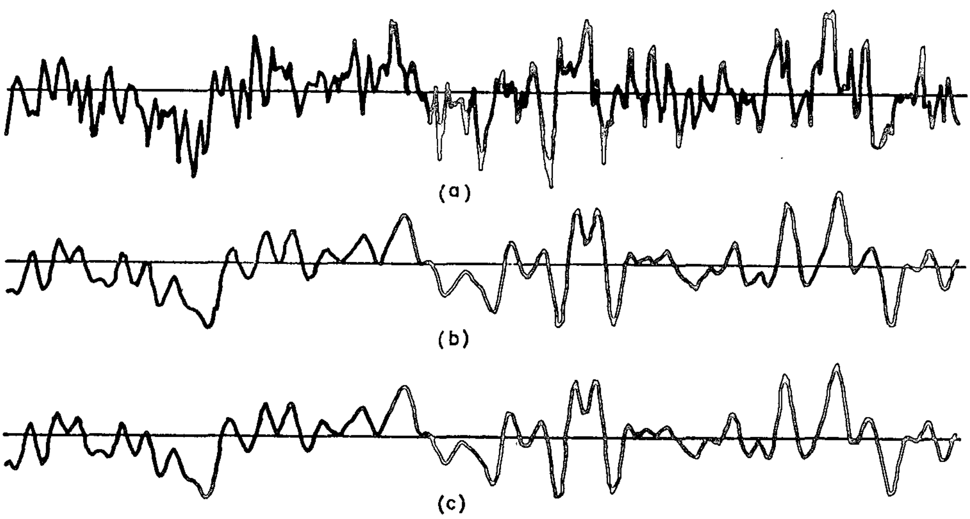

Fig. 5 Waveforms of (a) input signal (b) desired output signal (c) actual output signal of IIR LDMDF with leak factor β=0.984375.

low-pass digital filter. The sampling frequency of the DM was set to 128 kHz, that is, 16 times the Nyquist rate. The desired IIR filter was designed by the digital elliptic filter design program of Gray and Markel [8]. It has the following characteristics:

Passband cutoff frequency	1.2 kHz
Stopband cutoff frequency	1.8 kHz
Passband ripple	0.4 dB
Stopband attenuation	-40 dB.

Fig.4 shows the magnitude response of the IIR LDM filter with the characteristics specified above. In Fig.5, the performance of our IIR LDMDF is shown in the time domain. One can see from this figure that the actual output wave-form is the same as the desired ideal output waveform, indicating that the IIR LDMDF can be used as effectively as the conventional PCM filter.

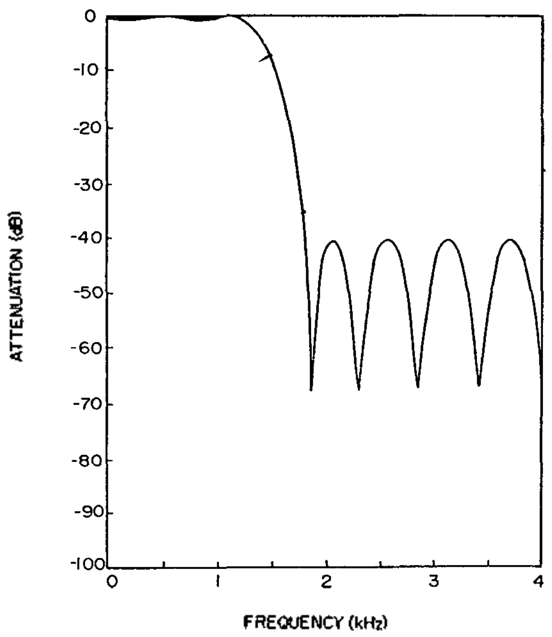

Fig. 6 Magnitude response of FIR LDMDF equivalent to that in Fig. 4.

Finally, let us compare the computation time of the IIR LDMDF realized in a direct form to that of the FIR LDMDF on the basis of the number of additions required for generation of one digital output. Here, we consider a type of FIR LDMDF in which analog input signal is sampled at the frequency of k times (in the present case k=16) the Nyquist rate, and digital outputs are generated at the Nyquist rate. Note that this kind of FIR LDMDF with M filter coefficients requires a storage of M words and Mk+1 additions for a digital output. Also, as described in the preceding section, the N-th order IIR LDMDF with B-bit wordlength requires two storages of 2^{N+1} and 2^N words, thus the total storage being equal to $3 \cdot 2^N$ words. It needs B+2 serial additions for a digital output. Also, note that the increases of the storage size and the number of adders reduce the computation time. Thus, we must compare the computation time of IIR and FIR LDMDF's on the equal basis, i.e., with the same storage size and the equal number of adders.

The filter coefficients for the FIR LDMDF were obtained by the FIR linear phase filter

Table I. Comparison of IIR (4-th order) and FIR LDMDF's.

	IIR	FIR	
		Type I	Type II
Storage	48	14	52
Number of additions	B+2	433	36

Note: B is the number of bits for filter coefficients.

design program of McClellan et al. [9]. With this program, the above specified constraints can be satisfied by having 27 filter coefficients.

The frequency response of this filter is shown in Fig.6. Taking into account that these FIR filter coefficients have a symmetric property, we need a storage of only 14 coefficients.

The storage size and the number of additions for the IIR and FIR LDMDF's under the above conditions are shown in Table I. The type I of FIR LDMDF was realized with a storage of 14 original filter coefficients, and the type II of FIR LDMDF was realized with the amount of storage and the number of adders equal to those of IIR LDMDF.

One can see from Table I that in the case of B=16, the computation time of the IIR LDMDF is one half of that of the equivalent FIR LD-MDF, and that in the case of B=8, it is approximately one third of that of the equivalent FIR LDMDF. Also, it should be noted that as the oversampling factor k increases for better output performance, and as the order of IIR LDMDF increases to meet more stringent constraints on the filter characteristics, the IIR LDMDF offers more significant saving in computation time.

Ⅳ. CONCLUSION

A method for realizing an IIR LDMDF has been presented. With this realization method, an IIR LDMDF can be implemented much simpler than the conventional PCM IIR digital filter, and offers much more saving in computation time than its equivalent FIR LDMDF. It should be emphasized that, although we have shown a low-pass IIR LDMDF as an example in this paper, the realization method presented can be used for design of other IIR LDMDF's such as high-pass, band-pass, and band-stop filters.

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