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OTA-Based Analog Multiplier Architecture

(OTA를 이용한 Analog Multiplier 구현에 관한 연구)

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要 約

아나로그 승산기를 구현하기 위하여 OTA를 회로의 기본요소로 사용하였다. OTA에서 일반적으로 나타나는 이동도 감쇄등의 비이상적인 현상을 두개의 OTA를 크로스 커플 형태로 사용함으로써 최소화 할 수 있음을 보였다. 실험적으로 90℃의 고온에서도 3차 고조파왜곡이 상쇄됨을 확인함으로써 OTA를 기본으로 하는 접근방식이 아나로그 신호처리에 적합함을 입증하였다.

Abstract

A building block approach to generate an analog multiplier architecture is described. Several non-idealities including the effects of the mobility degradation present in a typical operational transconductance amplifier (OTA) are minimized by using a two cross coupled OTA structure. It is shown that the third-order harmonic distortion is cancelled even at high temperatures. It is proved that OTA based approach is suitable for analog singal processing at relatively high temperatures.

I. Introduction

An analog multiplier [1-3]-[10,12] is a useful building block in many signal processing circuits. BJT analog multiplier has been used in modulators, wattmeters, and rms meters [4]. The lateral bipolar transistor in CMOS technology has also been used to implement a multiplier[5]. Recently, fully MOS analog multipliers have been proposed to be used as a building block in VLSI system. Most of the proposed approaches[1]-[3] are based on the well known Gilbert six transistor cell[6].

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A source-coupled differential input stage shown in Fig. 1 is widely used in op amp structures because it provides a high input impedance, large common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR), low dc offset voltage and noise. Assuming the simple square-law relationship, i.e., $I_D=K(V_{GS}-V_{TH})^2$, the drain currents for the transistors M1 and M2 become

$$I_{D1}=\frac{K}{2}\left(\sqrt{\frac{I_{ss}}{K}-\frac{V_i^2}{2}}+\frac{V_i}{\sqrt{2}}\right)^2 \quad (1)$$

$$I_{D2}=\frac{K}{2}\left(\sqrt{\frac{I_{ss}}{K}-\frac{V_i^2}{2}}-\frac{V_i}{\sqrt{2}}\right)^2 \quad (2)$$

where

$$K=\frac{\mu C_{ox}}{2}\cdot\frac{W}{L}$$

L, W=length and width of the gage

μ=carrier mobility

V_{TH}=threshold voltage of a MOSFET

C_{ox}=capacitance per unit area of the gate electrode.

Then, the output current, $I_{D_1}-I_{D_2}$, is found as

$$\Delta I=I_{D1}-I_{D2}=KV_i\sqrt{\frac{2I_{ss}}{K}-V_i^2} \quad (3)$$

When (3) is used for the Gilbert six transistor cell[5], the output current becomes

$$I_{out}=KV_x\left[\sqrt{\left(\sqrt{\frac{I_{ss}}{K}-\frac{V_y^2}{2}}+\frac{V_y}{\sqrt{2}}\right)^2-V_x^2}-\sqrt{\left(\sqrt{\frac{I_{ss}}{K}-\frac{V_y^2}{2}}-\frac{V_y}{\sqrt{2}}\right)^2-V_x^2}\right] \quad (4)$$

where V_x and V_y are the Gilbert Cell's inputs. To reduce the effects of the nonlinear terms (V_x^2) in the square roots of (4), predistortion techniques were used to linearize the output current[3]. By adding extra transistors, the output current can be linearized to some extend. However, there are two major factors causing deviations from the ideal square-law: the mobility degradation and transistors mismatch effects. Effects of these nonideal factors are analyzed in next section.

In this paper, operational transconductance amplifier (OTAs) are used as building blocks. An analog architecture based on OTA building blocks is proposed. It is shown that this architecture is simple and easy to implement. Furthermore, it has attractive properties such as minimum temperature dependence. The emphasis in this paper is in the proposed architecture, rather than in the OTA structure. Several improved OTA structures that can be used are disscused elsewhere [7]. An integrated prototype multiplier fabricated in standard 3μ CMOS process technology is presented. Experimental results agree well with expected theoretical results.

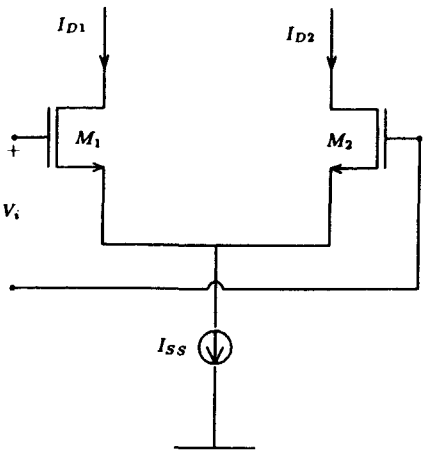


Fig.1. Source-coupled differential input stage

II. OTA-Based Analog Multiplier

The proposed block diagram of the multiplier is shown in Fig. 2. Inputs of the two OTAs are coupled as well as the outputs. Since one input signal, V_y is applied to the gate of a current source, the bias current, I_{SS}, of OTA1 becomes

$$I_{ss}=K_1(V_{bias}+V_y-V_{TH})^2 \quad (5)$$

The circuit schematic for the OTA blocks is illustrated in Fig. 3, with device sizes shown in Table 1. From (3) and Fig.3 the current difference between the input transistors of the differential amplifier of the OTA1 is given by

$$\Delta I_{DI}=I_{D_1}-I_{D_2}=K_1V_x\sqrt{\frac{2I_{ss}}{K_1}-V_x^2} \quad (6)$$

The current difference for the input stage of the OTA2 is

$$\Delta I_{DII}=I_{D4}-I_{D3}=-K_2V_x\sqrt{\frac{2I'_{ss}}{K_2}-V_x^2} \quad (7)$$

where

$$I'_{ss}=K_2(V_{bias}-V_{TH})^2$$

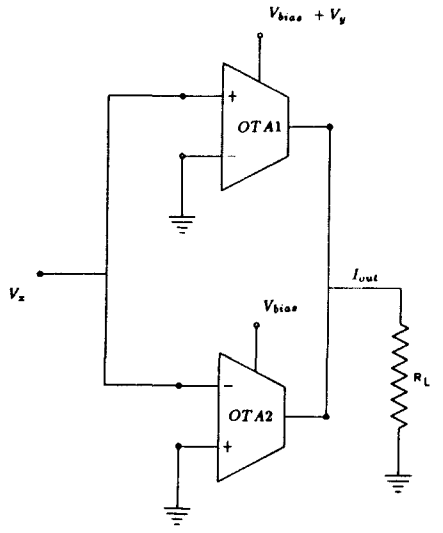


Fig.2. OTA-based analog multiplier.

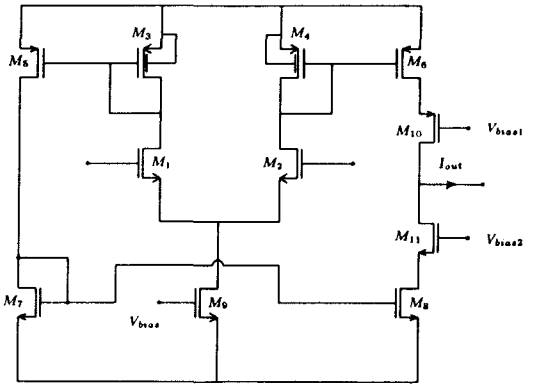


Fig.3. Schematic of the simple OTA.

Table 1. Device sizes of OTA block in μm.

MOSFETs	W	L
M_3, M_4, M_5	20	10
M_1, M_2	50	100
M_6	40	10
M_7	15	30
M_8	30	30
M_9	50	20
M_{10}	140	10
M_{11}	120	10

Then the total output current is expressed as

$$I_{out} = \{(I_{D1}-I_{D2})+(I_{D4}-I_{D3})\}A_{mir}$$
$$= (\Delta I_{D1}+\Delta I_{D11})A_{mir}$$
$$= K_1 V_x\left(\sqrt{\frac{2I_{ss}}{K_1}-V_x^2}-\sqrt{\frac{2I'_{ss}}{K_2}-V_x^2}\right)A_{mir} \quad (8)$$

where A_{mir} is a current mirror gain of transistors, M_4-M_6 and M_7-M_8. When the input voltage satisfy the inequalities $\frac{2I_{ss}}{K_1} > V_X^2$ and $\frac{2I'_{ss}}{K_2} > V_X^2$ and using Taylor Series expansion for the square root, (8) can be approximated as

$$I_{out} = K_1 V_x\left[\sqrt{\frac{2I_{ss}}{K_1}}-\Delta_1-\sqrt{\frac{2I'_{ss}}{K_2}}+\Delta_2\right] \quad (9a)$$

where $\triangle_1$ and $\triangle_2$ are the nonlinear deviation e.g.,

$$\Delta_1 \cong \frac{V_x^2}{2\sqrt{\frac{2I_{ss}}{K_1}}}-\frac{V_x^4}{8\sqrt{\left(\frac{2I_{ss}}{K_1}\right)^3}}-\cdots$$

Thus for $K_1 = K_2 = K$, (9a) yields

$$I_{out} \simeq KV_x\left[\sqrt{\frac{2I_{ss}}{K}}-\sqrt{\frac{2I'_{ss}}{K}}\right]$$
$$= KV_x\left[\sqrt{\frac{2K}{K}}\cdot(V_{bias}+V_y-V_T)-\sqrt{\frac{2K}{K}}(V_{bias}-V_{TH})\right]$$
$$= \sqrt{2}KV_xV_y \quad (9b)$$

In (9), note that the nonlinear terms $\triangle_1$ and $\triangle_2$ due to V_X^2 in the square root are not ignored but cancelled out for $K_1 = K_2$ at the output node by addition of the two output currents of each OTA. This multiplying method does not require extra circuits in order to linearize the transfer characteristic.

III. Effects of Nonidealities

Analyses in previous sections have been done with the assumption of an ideal square-law characteristic. But there are several effects causing deviations from the ideal square-law, mainly mobility degradation and transistors mismatch. It was shown[3] that mobility degradation causes

the third-order harmonic distortion, and mismatches cause output offset, second-order and higher-order nonlinearities. Let us consider the following nonidealities.

1. Effect of Mobility Degradation

Mobility degradation in a MOSFET can be modeled as

$$\mu = \frac{\mu_0}{[1+\theta(V_{GS}-V_{TH})]} \tag{10}$$

where θ is a process and temperature dependent parameter [9]-[10] When (10) is used in (1) and (2) for a source-coupled differential pair, the current difference can be expressed as

$$(I_{D1}-I_{D2}) = -K_1\theta V_i\left(\frac{I_{ss}}{K_1}-V_i^2\right)+ K_1V_i\sqrt{\frac{2I_{ss}}{K_1}-V_i^2} \tag{11}$$

also, we can wirte:

$$(I_{D4}-I_{D3}) = K_2\theta V_i\left(\frac{I'_{ss}}{K_2}-V_i^2\right)+ K_2V_i\sqrt{\frac{2I'_{ss}}{K_2}-V_i^2} \tag{12}$$

It is noticeable that the mobility degradation effect on OTA1 has the same magnitude but opposite sign as of OTA2. As was shown in [3], the first terms in (11) and (12) cause the third harmonic distortion. So when (11) and (12) are substituted into (8) the nonlinear terms are cancelled at the output node, consequently, third-order harmonic distortion can be ideally eliminated for $K_1=K_2$.

2. Effect of Transistor Mismatches

For actual fabrication, the MOSFET's active areas are defined by several different masks, such as poly mask and diffusion mask, therefore random length and width variations between devices should be expected. As shown in Fig. 3, a CMOS OTA basically consists of three current mirrors and a differential input stage. To simplify analysis of the statistical mismatch of transistors, each block is analyzed separately; the current mirror block and the differential pair block. For simplicity, only geometrical and threshold voltage mismatches are considered here.

1) Mismatch in current mirrors

Let us consider a conventional current mirror as shown in Fig. 4. A simple square law is also assumed for the drain currents. Effect of process variation can be found by including statistical parameters, $\triangle\left(\frac{W}{L}\right)$ and $\triangle V_{TH}$ as

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)+\frac{\Delta\left(\frac{W}{L}\right)}{2} \tag{13a}$$

$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)-\frac{\Delta\left(\frac{W}{L}\right)}{2} \tag{13b}$$

$$V_{TH1} = V_{TH}+\frac{\Delta V_{TH}}{2} \tag{13c}$$

$$V_{TH2} = V_{TH}-\frac{\Delta V_{TH}}{2} \tag{13d}$$

Then, the ratio of two currents in the worst case is expressed as

$$\frac{I_{out}}{I_{in}} = \frac{\left(\frac{W}{L}\right)_2(V_{GS}-V_{TH2})^2}{\left(\frac{W}{L}\right)(V_{GS}-V_{TH1})^2} = \frac{\left(\frac{W}{L}-\frac{\Delta\left(\frac{W}{L}\right)}{2}\right)\left(V_{GS}-V_{TH}+\frac{\Delta V_{TH}}{2}\right)^2}{\left(\frac{W}{L}+\frac{\Delta\left(\frac{W}{L}\right)}{2}\right)\left(V_{GS}-V_{TH}-\frac{\Delta V_{TH}}{2}\right)^2} \tag{14}$$

And reasonable assumptions

$$\frac{\Delta\left(\frac{W}{L}\right)}{2\left(\frac{W}{L}\right)} \ll 1, \quad \frac{\Delta V_{TH}}{2(V_{GS}-V_{TH})} \ll 1 \tag{15}$$

reduce (14) to

$$\frac{I_{out}}{I_{in}} \simeq 1-\frac{\left(\frac{W}{L}\right)\Delta}{\frac{W}{L}}+\frac{2\Delta V_{TH}}{(V_{GS}-V_{TH})} \tag{16}$$

The second term is geometry dependent and the third term is threshold voltage and bias point dependent. The variation of the threshold voltage

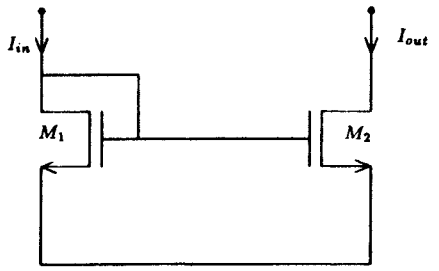


Fig.4. Simple current mirror.

$\triangle V_{TH}$ can be reduced by building two transistors in a common-centroid structure with resulting standard deviations on the order of 2mV range [11].

2) Transistor Mismatch in the Differential Pair

To determine the effect of transistor mismatches, let us start with the square-law characteristic in the source coupled pair. Two drain currents and input voltage are related as

$$I_{D1}+I_{D2}=I_{ss} \tag{17a}$$

$$\sqrt{\frac{I_{D1}}{K_1}}-\sqrt{\frac{I_{D2}}{K_2}}=V_i \tag{17b}$$

Thus I_{D_1} can be expressed as

$$I_{D1} = \frac{-\left[(K_2V_i^2-I_{ss})\left(1+\frac{K_2}{K_1}\right)-2K_2^2\frac{1}{K_1}V_i^2\right]}{\left(1+\frac{K_2}{K_1}\right)^2}+ \frac{\sqrt{(K_2V_i^2-I_{ss})\left(1+\frac{K_2}{K_1}\right)-2K_2^2\frac{1}{K_1}V_i^2-\left(1+\frac{K_2}{K_1}\right)^2(K_2V_i^2-I_{ss})}}{\left(1+\frac{K_2}{K_1}\right)^2} \tag{18a}$$

$$= \frac{K_1}{K_1+K_2}\left[I_{ss}-\frac{K_2-K_1}{K_1+K_2}\cdot K_2V_i^2+ V_i\sqrt{\frac{2I_{ss}\cdot 2K_1K_2}{(K_1+K_2)^2}-\frac{4K_1K_2^2}{(K_1+K_2)^2}V_i^2}\right] \tag{18b}$$

Now, consider a mismatch effect expressed as

$$K_1=K+\Delta K \tag{19a}$$

$$K_2=K-\Delta K \tag{19b}$$

Equation (18b) can be simplified

$$I_{D1}=\frac{I_{ss}}{2}-\frac{\Delta K}{2K}I_{ss}+\frac{\Delta K}{2}V_i^2+ \frac{K}{2}V_i\sqrt{\frac{2I_{ss}}{K}-V_i^2} \tag{20}$$

Similar expression is obtained for I_{D2} as

$$I_{D2}=\frac{I_{ss}}{2}+\frac{\Delta K}{2K}I_{ss}-\frac{\Delta K}{2}V_i^2+ \frac{K}{2}V_i\sqrt{\frac{2I_{ss}}{K}-V_i^2} \tag{21}$$

which is the same expression as (3) when $\triangle K=0$. From (20) and (21), the output current $\triangle I$ yields

$$\Delta I=\frac{\Delta K}{K}I_{ss}-\Delta KV_i^2+KV_i\sqrt{\frac{2I_{ss}}{K}-V_i^2} \tag{22}$$

This is a general expression of K mismatch effect for the source-coupled differential pair. In equation (22), first and second terms cause the offset and second harmonic distorition, respectively.

IV. Experimental Results

Multiplier of Fig. 2 has been fabricated in a CMOS p-well 3μ double-poly technology by MOSIS. Fig. 5 shows the die photographs of the test multiplier. The entire multiplier, including the several test devices and on-chip output buffer occupies an area of 1800 x 100 μm^2. Fig. 6 shows the performance of the realized multiplier as a frequency doubler. Fig. 7 shows the structure as a modulator with the input frequencies for

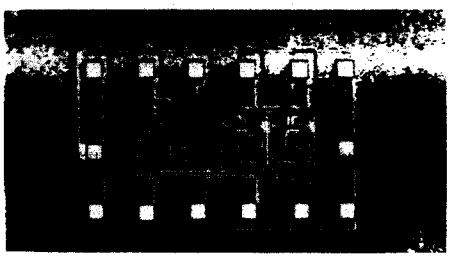


Fig.5. Photograph of fabricated multiplier using p-well 3μ double-poly technology.

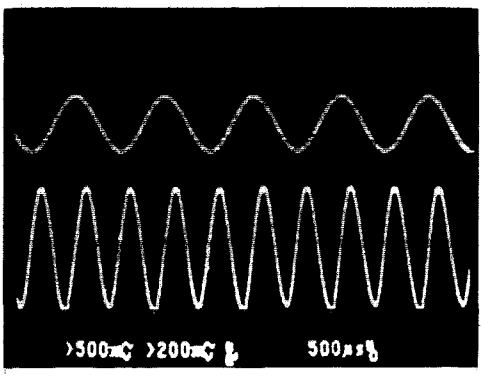
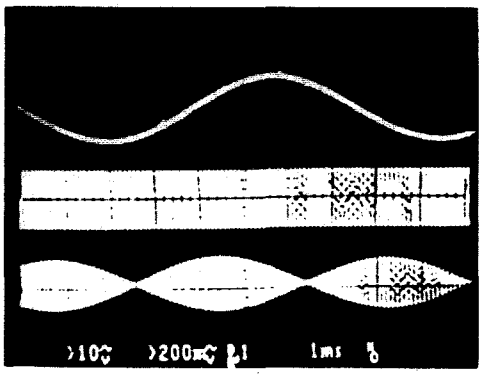
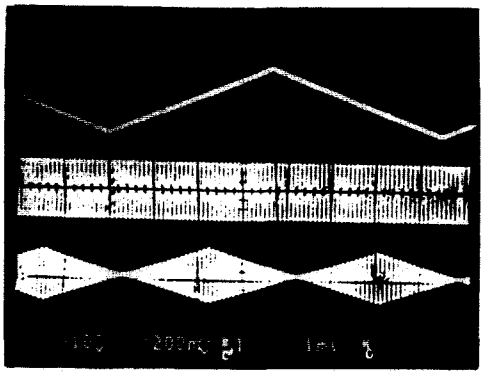


Fig.6. Multiplier as a frequency doubler with 200mV input at 2kHz.



a) max$|V_x|$=V and max$|Vy|$=V



b) max $|V_x|$=max and max$|V_y|$=V

Fig.7. Modulator. Input frequencies for input V_x=1 kHz and for input V_y=11 kHz, respectively.

V_x=1kHz and V_y=11kHz, respectively. Also output signal spectrum are shown in Fig. 8 which

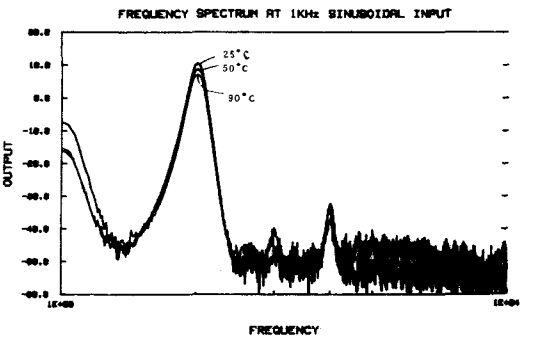


Fig.8. Spectral characteristics at 25°, 50°, and 90°C.

are measured at three different temperatures, 25°, 55°, and 90°C and the fundamental frequency of 2kHz. Results of spectral performances at the three different temperatures are summarized in Table 2. These experimental results show that the multiplier has a temperature factor of about 2600 ppm/°C. Note that third-harmonic does not appear even at 90° C. Maximum peak to peak input signals at V_x and V_y are 350 mV_{PP} and 250 mV_{PP}[2], respectively . Dynamic range is measured to be 67 dB which is good enough for many applications. Realized multiplier dissipates 5 mW at 100 μA bias current. Experimental data is surmmarized in Table 3.

IV. Conclusions

A building block approach to generate an analog multiplier architecture has been described. Nonidealities due to the mismatches of differential pair and current mirrors, and the effect of mobility degradation are analyzed. It is shown that the third harmonic distortion can be reduced

Table 2. Spectral Characteristics at Different Temperatures.

Temp.	I_{bias}	Fundamental Deviations (%)		2nd Harmonic	3rd Harmonic
25°C	50μ	9.8dB	–	-32.5dB	–
55°C	50μ	9.1dB	7.14	-33.2dB	–
90°C	50μ	8.2dB	16.3	-34.1dB	–

Table 3. Summary of the integrated multiplier performance.

Maximum Input Voltage for 1% THD	V_x 350 mV V_y 250 mV
Dynamic Range	67 dB
3 dB Bandwidth	70 kHz
Offset Voltage	500 μV
PSRR	53 dB at 10kHz
Power dissipation	5 mW

by using across coupled OTA block architecture. Applicability of integrated multiplier to high temperatures has been demonstrated. Experimental data confirm the validity of the analysis.

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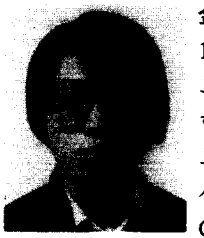

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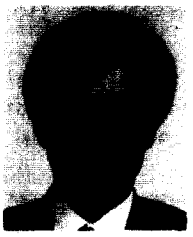

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