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The TDDB Characteristics of Thin SiO_2 with Stress Voltage Polarity

(스트레스전압 극성에 따른 얇은 산화막의 TDDB 특성)

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(Cheon Soo Kim, Kyoung Soo Yi, Kee Soo Nam and Jin Hyo Lee)

要 約

얇은 산화막의 신뢰성을 정전류 스트레스 방법으로 조사하였다. 실험에 사용된 소자는 산화막 두께가 20~25nm인 다결정실리콘 MOS 커패시터 이었다. VLSI 신뢰성 평가에 필수적인 자동측정 및 통계적 데이타분석을 HP 9000 컴퓨터를 이용하여 수행하였다. 측정한 TDDB 결과로부터 산화막의 결함밀도, 절연파괴 전하량(Qbd), 수명등을 측정한 결과 스트레스를 가하는 극성에 따라서 다른 특성이 나타났다. 결함밀도는 (−) 게이트 주입의 경우에 62개/cm^2이었다. 절연파괴 전하량은 (+) 게이트 주입의 경우 30C/cm^2 이었고, (−)게이트 주입의 경우 21C/cm^2이었다. 또한 전류밀도 가속인자(current density acceleration factor)는 (−) 게이트 주입의 경우가 1.43cm^2/A이었고, (+) 게이트 주입의 경우가 1.25cm^2/A이었다.

Abstract

The reliability of the thin thermal oxide was investigated by using constant current stress method. Polysilicon gate MOS capacitors with oxide thickness range of 20-25 nm were used in this experiment. Automatic measurement and statistical data analysis which were essential in reliability evaluation of VLSI process performed by HP 9000 computer. Based on TDDB results, defect density, breakdown charge (Qbd) and lifetime of oxide film were evaluated. According to the polarity of the stress, some different characteristics were shown. Defect density was 62/cm^2 at negative gate injection. The value of Qbd was about 30 C/cm^2 at positive gate injection, and about 21 C/cm^2 at negative. The current density acceleration factor was 1.43 cm^2/A for negative gate injection, and 1.25 cm^2/A for positive gate injection.

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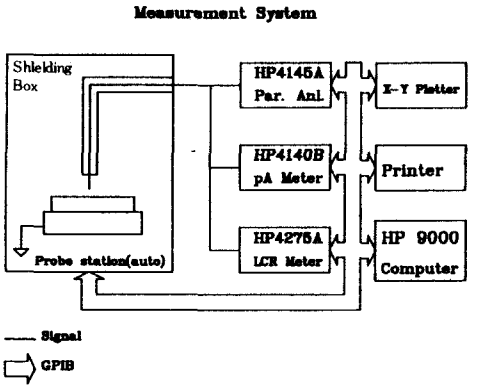
I. Introduction

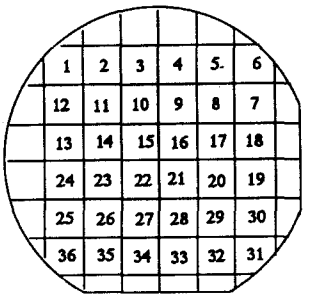
Time dependent dielectric breakdown (TDDB) characteristics has been recognized as one of the major failure modes for MOS integrated circuits. As the gate oxide thickness reduces less than

100 Å, oxide breakdown reliability will become more serious problem. While much works have been done on the TDDB of gate oxides, the reported breakdown acceleration factors(β) scattered over a wide range [1, 2]. The disagreement of regarding acceleration factor is not well understood. Charge to breakdown (Qbd) value has the dependence of oxide thickness and stress voltage polarity [3-5]. Stress voltage polarity dependence, breakdown mechanism of thin gate oxide still remain unclear. Oxide reliability under negative gate stress has not been throughly examined yet, because n-channel device operated by positive voltage is widely used for VLSI's.

In this study, the reliability of the thin thermal oxide was investigated by using constant current stress method. The thickness range of oxide was 20-25 nm. Defect density and current acceleration factor (β) of oxide film were analyzed with the polarity of stress voltage. Using the acceleration factor, lifetime of oxide films under normal operating condition were evaluated by extrapolation of the high current accelerated test data. To explain the cause of TDDB, oxide trapped charge (Qot) and interface trapped charge (Qit) quantity was measured by C-V, I-V method.



(a)



(b)

Fig.1. (a) Block diagram of measurement system.
(b) Data input with mouse in wafer mapping program.

II. Experiment

The MOS capacitors used in this study were fabricated on 5-inch (100) silicon wafers by using the conventional n-well CMOS process. A gate oxide layer with thickness range of 20-25 nm was thermally grown in O_2 + TCA ambient at 1000°C. A poly-silicon film with a thickness of 3000 Å was deposited on the oxide layer using the LPCVD at 625°C and then doped with phosphorus dopant using a $POCl_3$ source. After depositing aluminum, the aluminum film was etched. Finally the wafers were alloyed in forming gas at 450°C for 30 min.

III. Measurement

Fig. la shows schematic diagram of measurement system. A constant current was applied to the MOS capacitors using HP 4145 semiconductor parameter analyzer. The voltage acrossing the capacitor, which is necessary for the constant current, was monitored with time variable. When the breakdown of capacitor occurred, the voltage across the capacitor drops abruptly. The breakdown time of the capacitor was stored as a data. After the measurement point moving on wafer, next measurements performed automatically. Fig. 1b shows the randomly selected chips to be measured. All these procedure performed by HP 9000 computer. Fig. 2. shows the block diagram of auto-TDDB measurement program.

To study charge trapping mechanism, after the known interval of stress, high-frequency C-V and quasi-static C-V were measured with HP 4275 LCR Meter and HP 4140B pA Meter, respectively. Flat band voltage (Vfb) shift and interface trap density (Dit) were also measured with stress time.

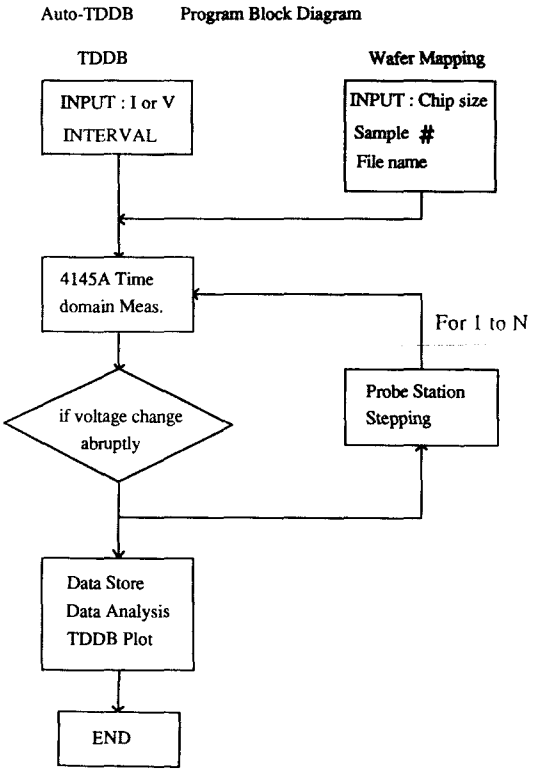


Fig.2. Block diagram of automatic TDDB measurement program.

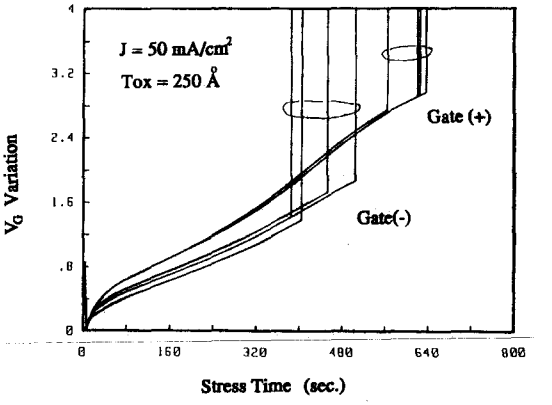


Fig.3. Voltage variation across the capacitor for constant current as a function of stress time.

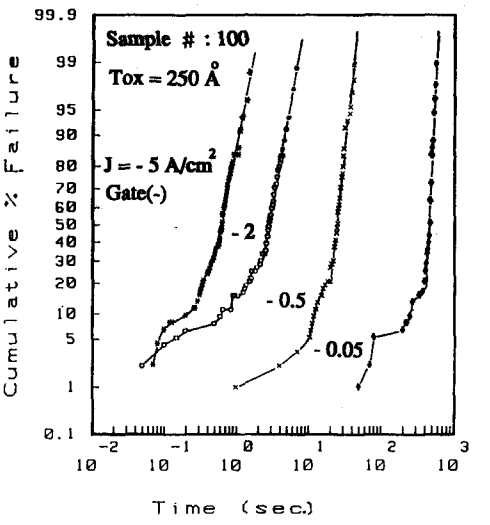


Fig.4. TDDB Characteristics of 25nm oxide film under several current density stress. stress were applied negative gate polarity.

IV. Results and Discussions

1. *TDDB Characteristics with Gate stress polarity*

The voltage variation needed to maintain a constant current through the oxide as a function of the stress time is shown in Fig. 3. The device stressed at a current density of 50 mA/cm^2. The gate voltage decrease initially then increase with time until breakdown. The increase in gate voltage necessary to maintain a constant current is due to electron trapping in the SiO_2 [6]. In addition, breakdown charge (Qbd) of a 25nm oxide for positive gate injection was about 30 C/cm^2, which is much greater than that of negative gate injection.

Fig. 4. shows the results of the TDDB measurement. Hundred MOS capacitors were tested under several current density, and cumulative percentage failure was plotted on a log normal chart as a function of the breakdown time. It can be seen that the distribution is composed of two distinct sloped, related to intrinsic breakdown and defect-related breakdown. We also changed the log-normal distribution to Weibull distribution form to evaluate defect density [7]. The calculated defect density was 62/cm^2.

Fig. 5 shows the result of the TDDB measurement. Same as a Fig. 4 except the gate injection polarity. It can be seen that the distribution

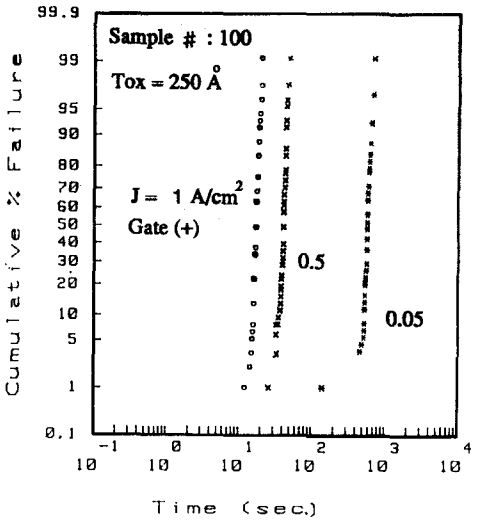


Fig.5. TDDB Characteristics of 25nm oxide film under several current density stress. Stress were applied positive gate polarity.

hardly disperses and the straight line can be obtained without the defect related breakdown distribution. This indicates that nearly no electrically weak spot to cause breakdown. The cause of the dissimilar distribution of breakdown time with gate injection polarity is that the polisilicon/SiO_2 interface may be weaker than Si/SiO_2 [4].

To determine the electrical accerlation factor of TDDB, the time to reach 50% cumulative failure is plotted as a function of the stress current density in Fig. 6. The time to 50% failure increases logarithmically with the atress current density. From the slope of these lines, we obtained the current density acceleration factors (β). The value of β was 1.43 (cm^2/A) for negative gate injection and 1.25 (cm^2/A) for positive gate injection. These values are well consistent with the previous paper [13]. With these results, we can expect the lifetime of oxide films under low current density. The expected lifetime and accleration factor are listed in Table 1.

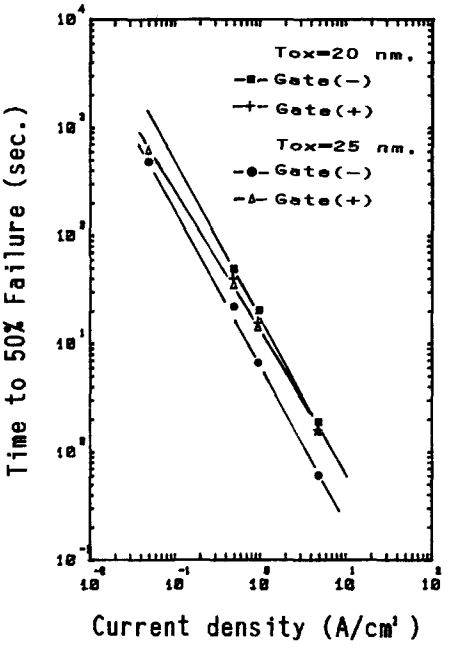


Fig.6. Time to reach 50% failures as a function of current density for 20nm and 25nm SiO_2 films.

Table 1. Current acceleration factor and extrapolated lifetime of SiO_2 films with gate stress polarity.

Tox	Gate stress Polarity	Current Acceleration factor (β) cm^2/A	Extrapolated lifetime at J=1E-6 A/cm^2
200Å	(+)	1.25	6E9 sec.
	(−)	1.43	8E8 sec.
250Å	(+)	1.25	8E8 sec.
	(−)	1.43	2E9 sec.

2. Charge trapping and TDDB mechanism

To clarify the charge trapping and TDDB mechanism, C-V and I-V were measured before and after the TDDB stress. Fig.7 and Fig. 8 show high frequency C-V curve after several stress times for 25 nm film capacitor stressed at 1mA/cm^2 and -12.5 mA/cm^2, respectively. (- refers to current injection from the polisilicon gate, and + refers to injection from the silicon substrate) As shown in Fig. 7, initially flat band voltage shifts to negative value of gate bias with respect to initial flat band voltage, then move to positive value with stress time. This means that positive charges are generated initially in the bulk of the oxide, followed by negative ones with stress time [8]. In addition, C-V cure not deformed, only shift

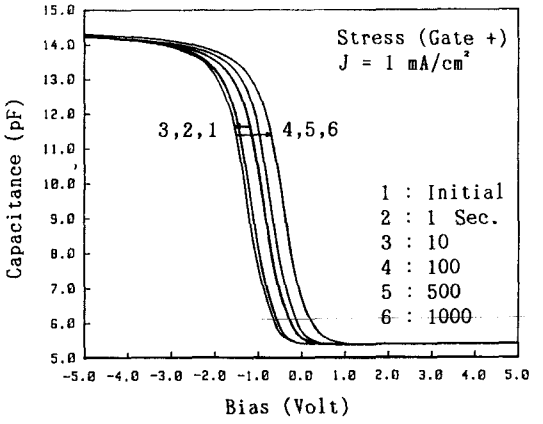


Fig.7. High frequency C-V plot as a parameter of stress time. Stress condition were 1 mA/cm^2.

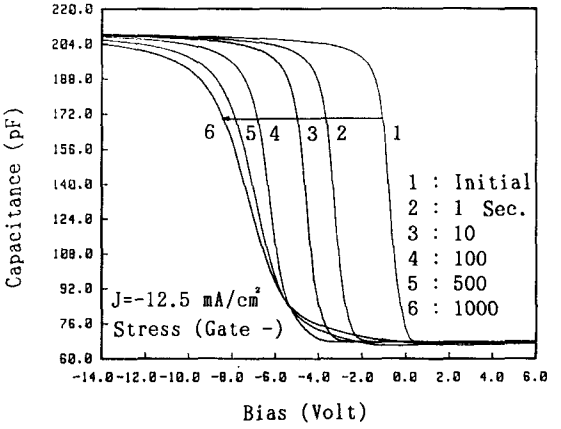


Fig.8. High frequency C-V plot as a parameter of stress time. Stress condition were -1 mA/cm^2.

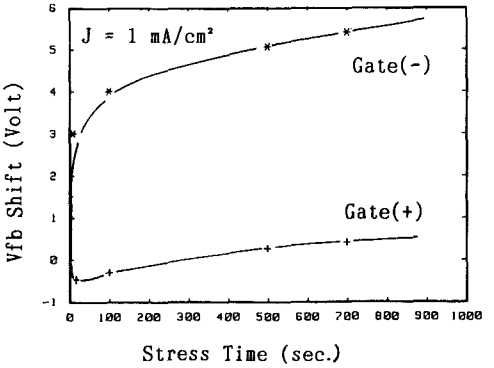


Fig.9. Flat band voltage shift as a function of stress times.

parallel direction which means that the charges are all trapped in the bulk of oxide. For negative gate injection, flat band voltage only shifts to negative value of gate bias, and deformation of C-V curve was observed (Fig. 8) which means that interface states were also generated in the Si/SiO_2 interface with the stress time. Fig. 9 shows the flat band voltage shifts with the gate injection polarity as a function of the stress time.

Fig. 10 and Fig. 11 show quasi-static C-V curve of the capacitor after the several stress times stressed at 1 mA/cm^2 and -1 mA/cm^2, respectively In addition to the oxide trapped charge, interface

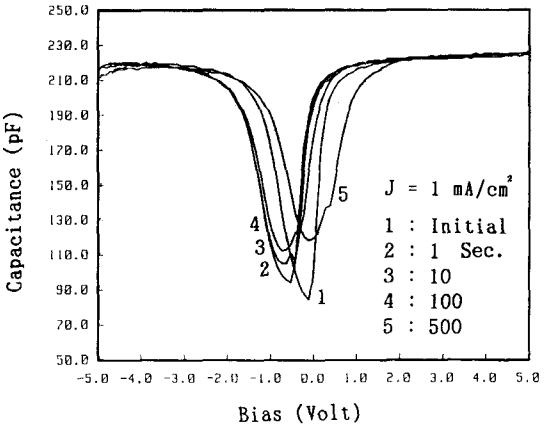


Fig.10. Quasi-static C-V plot as a parameter of stress times. Stress condition were 1 mA/cm^2.

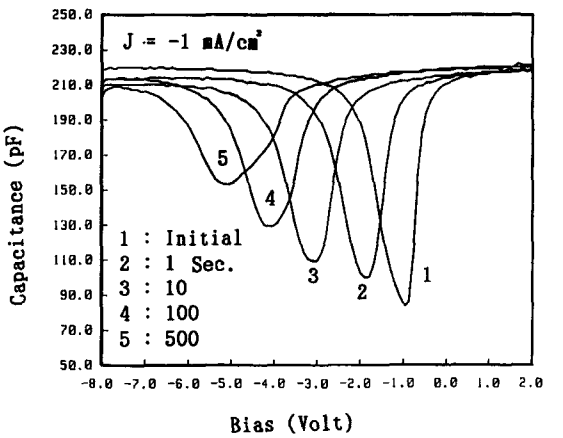


Fig.11. Quasi-static C-V plot as a parameter of stress times. Stress condition were -1 mA/cm^2.

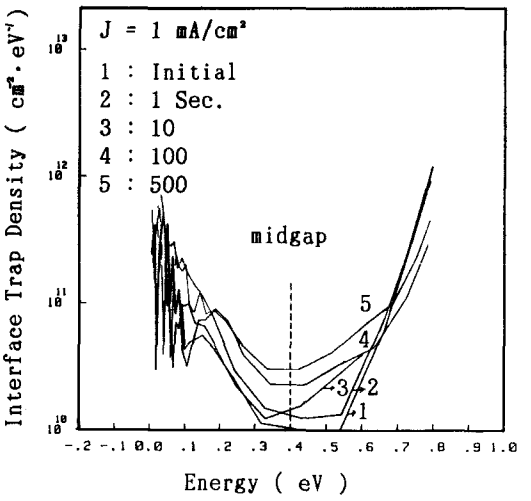


Fig.12. Interface trap density distribution as a parameter of stress time. Stress condition were 1 mA/cm^2.

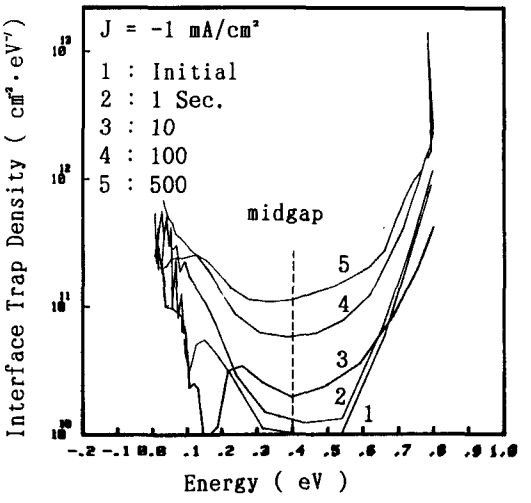


Fig.13. Interface trap density distribution as a parameter of stress time. Stress condition were -1 mA/cm^2.

state charges were also generated at Si/SiO_2 interface during the stress. The interface state density distributions, calculated from these curves, are plotted in Fig. 12 and Fig. 13. Interface state density increased over the entire bandgap with stress time. For negative bias stress, as shown in Fig. 14, interface trap density existing at midgap

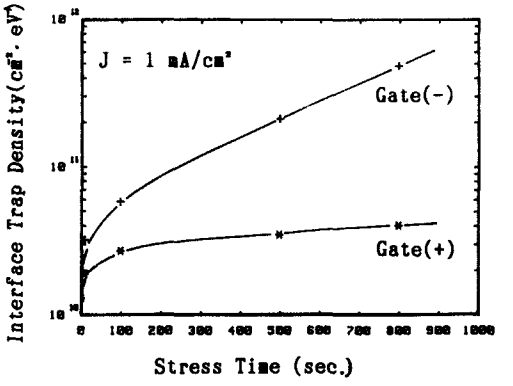


Fig.14. Interface trap density as a function of stress times.

region was 5-6 times greater than that of positive bias stress under the same current density. Based on these trap charges in the SiO_2 films, TDDB mechanism with gate polarity is discussed. For positive voltage stress, small positive charge and interface trap were generated initially, and then negative charge trapping followed at the anode as shown in Fig. 9 and Fig. 14. But interface state density saturated at certain value. The negative charge at cathode enhenced the injection current, then electrical breakdown occured at weak spot of the gate area [19-11]. For negative voltage stress, many positive charges and interface charges are produced. Much greater number of negative charges and interface charges are generated in the case of positive stress [12]. Negative voltage stressing differs from positive voltage stressing in that the interface state density was 5-6 times greater at the same injection current density. The positive charge produced at cathode increased the electric field and leading to dielectric breakdown. The reason for shorter lifetimes on negative voltage TDDB stress was closely related these results.

V. Conclusions

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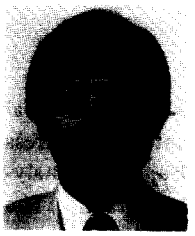

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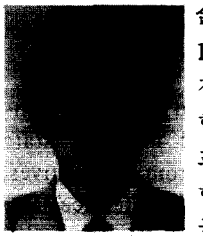

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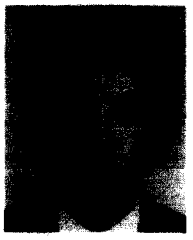

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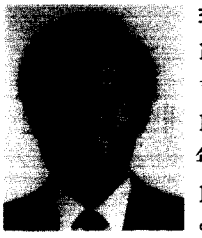

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