論 文

Parallel Scrambling Techniques for SDH and ATM Transmissions

Seok Chang Kim*, Byeong Gi Lee* *Regular Members*

SDH와 ATM 전송을 위한 병렬혼화 기법

正會員 金 錫 昌* 正會員 李 秉 基*

ABSTRACT

In this paper, parallel scrambling techniques are considered for practical use in the SDH transmission and the ATM transmission. In the ATM transmission, there are two ways of transmitting ATM cells – the SDH-based and the cell-based – and the corresponding scrambling techniques differ accordingly. For the SDH transmission and the SDH-based ATM transmission, the FSS(frame synchronous scrambling) is applied to the STM frames; while for the cell-based ATM transmission, the DSS(distributed sample scrambling) is used on the ATM cell stream. The parallel scrambling techniques are examined for the FSS and the DSS, and applied to achieve the parallel FSSs for use in the SDH and the SDH-based ATM transmission along with the parallel DSS applicable to the cell-based ATM transmission. The resulting(8,4) PSRG(parallel shift register generator) and (8,16) PSRG based parallel scramblings are directly applicable for the STM-1 rate processing of the STM-4 and STM-16 scramblings, respectively. Likewise, the resulting (1,8) PSRG and double-sampling-double-correction based parallel scrambling techniques can be practically used for a low-rate processing of the SDH-based and the cell-based ATM signal scrambling respectively.

I. Introduction

In today's lightwave transmission, information data can be transmitted via two typical transmission systems : One is the *SDH(Synchronous Digital Hierarchy) transmission system* and the other is the *ATM(Asynchronous Transfer Mode) transmission system*, both of which have been standardized by CCITT [1][2]. In the SDH system[1], information data are synchronously mapped into STM (Synchronous Transport Module) frames, which are scrambled by the *FSS(Frame Synchronous Scrambling)* before transmission. The transmission rates of the signals STM-1, STM-4 and STM-16 are respectively 155.520 Mbps, 622.080(=4×155.520) Mbps and 2488.320(=16×155.520) Mbps.

In the ATM system[2], information data are

*서울大學校 電子工學科
Dept. of Elec. Eng., Seoul Univ.
論文番號 : 93-118

asynchronously mapped into ATM cells, which can be transmitted via two ways of transmission, the *SDH-based transmission* and the *cell-based transmission*. For the SDH-based ATM transmission, ATM cell stream is self-synchronously scrambled, and then mapped into the STM frame STM-1 or STM-4. The STM frames are also scrambled by the same FSS used for the SDH transmission system. On the other hand, for the cell-based ATM transmission, ATM cell stream is scrambled by the *DSS(Distributed Sample Scrambling)*, and then directly transmitted. The transmission rates of the cell-based transmission can also be 155.520 Mbps or 622.080 Mbps like the SDH-based case.

The scrambling techniques, FSS and DSS, are similar in that they scramble and descramble the transmission signals by adding SRG(shift register generator) sequences to the raw data streams. But the two are different in the method of synchronizing the state of the descrambler SRG to that of the scrambler SRG. In the FSS[3], the scrambler and the descrambler SRGs are synchronized by resetting the states of both SRGs to a prespecified state at the start of each frame; while in the DSS [2][4][5], some samples taken from the scrambler SRG state are transmitted to the descrambler SRG, which are used for correction of the descrambler SRG state. For the DSS, the sampling conditions of the scrambler SRG state and the correction conditions of the descrambler SRG state are reported in [4] through [7].

Since scrambling is a bit-level signal processing performed immediately before transmission, the scrambling rates are identical to the corresponding transmission rates. That is, the scrambling rate is 155.520 Mbps, 622.080 Mbps, or 2488.320 Mbps for the SDH transmission, and 155.520 Mbps or 622.080 Mbps for the ATM transmission. Therefore these high transmission rates impose techological burdens on the implementations of scrambling. Moreover, in the case where the transmission rates extend much higher, scrambling at such high transmission rates may be impossible due to the limits of existing technology.

To combat this scrambling rate problem, the concept of *parallel scrambling* has been introduced, which enabled us to perform the scrambling process at the low-speed base-rate [8]. As opposed to this, the conventional transmission-rate scrambling process is called *serial scrambling*. Under the parallel scrambing, a set of scrambling process is performed at the base rate, collectively achieving the effect of the serial scrambling at the transmission rate.[1]

In the case of the FSS, parallel scrambling techniques for the bit-interleaved multiplexing environment can be found in [8]. Recently a theory on *PSRG(parallel shift register generators)* has been developed [10][11][12], which makes parallel FSSs extensible for multibit-interleaved multiplexing environments. On the other hand, in case of the DSS, the *double sampling* and the *double correction* conditions has been developed for parallel realizations of DSSs [13].

In this paper, we will show how to apply the parallel scrambling techniques for practical use in the SDH and ATM transmission systems of today's optical networks and BISDN(Broadband Integrated Services Digital Network). In Section Ⅱ we will first review the PSRG theory for parallel FSSs, and in Section Ⅲ we will review the double sampling and correction conditions for parallel DSSs. Using these parallel scrambling techniques, we will then consider the parallel FSS for use in the SDH transmission system in Section Ⅳ. Finally, in Section Ⅴ we will examine the parallel FSS and the parallel DSS respectively for applications to the SDH-based and cell-based ATM transmission systems.

1. The parallel scrambling techniques can also be combined with the permuting techniques to be applied for signal alignments in rolling-based lightwave transmission [9].

Ⅱ. Parallel Scrambling Techniques for FSS[2]

Shift register generators(SRG) can be classified into two categories : *SSRG*(Simple SRG) and *MSRG*(Modular SRG). An SSRG is determined by its *characteristic polynomial*

$$C(x)=\sum_{i=0}^{L} c_i x^i, \tag{1a}$$

and an MSRG is determined by its *generating polynomial*

$$G(x)=\sum_{i=0}^{L} g_i x^i, \tag{1b}$$

where the *SRG length* L is the number of shift registers, and the coefficients c_i and g_i are either 0 or 1 for $i=1, 2, \cdots, L-1$, and are both 1 for $i=0$ and L.

Fig.1 shows configurations of the SSRG and the MSRG characterized by equations (1a) and (1b) respectively. In the figure, each rectangular block indicates a shift register ; the value $d^c_{i,k}$ or $d^g_{i,k}$ inside the block represents the kth state value of the shift register ; and the sequences $\{t_k,\ k=0,\ 1,\ \cdots\}$ and $\{s_k,\ k=0,\ 1,\ \cdots\}$ are called the *SSRG and MSRG sequences* respectively.

The *kth state polynomials* $D^c_k(x)$ and $D^g_k(x)$ are the polynomials representing the shift register states at time k for the SSRG and the MSRG respectively, that is,

$$D^c_k(x)=\sum_{i=0}^{L-1} d^c_{i,k} x^i, \tag{2a}$$

$$D^g_k(x)=\sum_{i=0}^{L-1} d^g_{i,k} x^i. \tag{2b}$$

The 0th state polynomials $D^c_0(x)$ and $D^g_0(x)$ are called the *initial state polynomials* of the SSRG and the MSRG sequences respectively. Then, an SSRG sequence $\{t_k\}$ is completely determined by its characteristic polynomial $C(x)$ and its initial state polynomial $D^c_0(x)$; and an MSRG sequence $\{s_k\}$ is completely determined by its generating polynomial $G(x)$ and its initial state polynomial $D^g_0(x)$. Therefore, an SSRG sequence $\{t_k\}$ is denoted as $S_{SSRG}[C(x),\ D^c_0(x)]$ and an MSRG sequence $\{s_k\}$ is denoted as $S_{MSRG}[G(x),\ D^g_0(x)]$.

For the SSRG sequence $S_{SSRG}[C(x),\ D^c_0(x)]$ and the MSRG sequence $S_{MSRG}[G(x),\ D^g_0(x)]$, if $C(x)$, $D^c_0(x)$, $G(x)$ and $D^g_0(x)$ satisfy the relations

$$C(x)=x^L G(x^{-1}), \tag{3a}$$

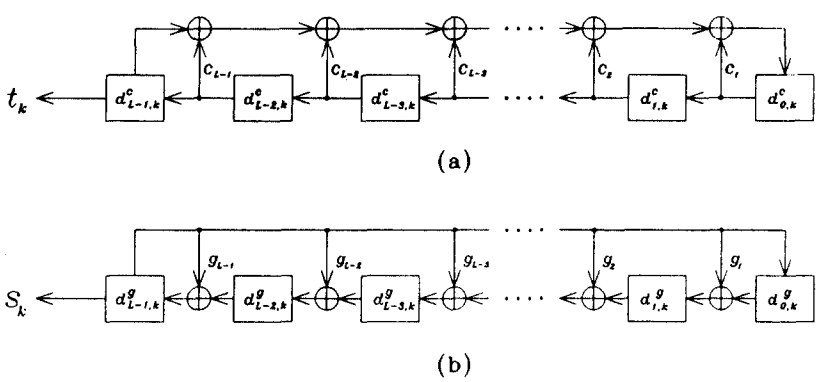

Fig. 1. Shift register sequence generator.
(a)SSRG, (b)MSRG.

2. For a more detailed description on this, refer to [10], [11] and [12].

$$D_0^c(x)=Q[G(x),\ x^L D_0^g(x)], \tag{3b}$$

then the two sequences are identical to each other.[3,4]

For a given sequence $\{s_k\}$, an (M, N) *PSRG(Parallel Shift Reigister Generator)* is an SRG which generates N *parallel sequences* T_i, $i=0, 1, \cdots, N-1$, meeting the relations

$$\begin{aligned}
T_0&=\{s_0, \cdots, s_{M-1}; s_{MN}, \cdots, s_{M(N+1)-1}; \cdots\},\\
T_1&=\{s_M, \cdots, s_{2M-1}; s_{M(N+1)}, \cdots, s_{M(N+2)-1}; \cdots\},\\
&\cdots\cdots\cdots\cdots\\
T_{N-1}&=\{s_{M(N-1)}, \cdots, s_{MN-1}; s_{M(2N-1)}, \cdots, s_{2MN-1}; \cdots\}.
\end{aligned} \tag{4}$$

In other words, an (M, N) PSRG for a sequence generates N parallel sequences such that the *M-bit interleaved* sequence, which is obtained by interleaving them by M sequence elements(or M *bits*), is identical to the original sequence. Fig.2 describes an (M, N) PSRG for a sequence $\{s_k\}$.

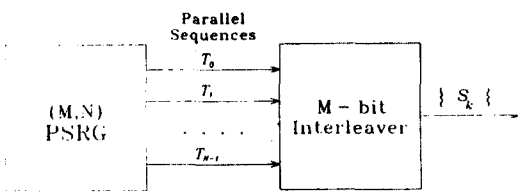

Fig. 2. An (M,N) PSRG for a sequence $\{s_k\}$.

The (M, N) PSRG sequences T_i's in (4) can be obtained by the decimation and interleaving of sequences. More specifically, we first MN-decimate the sequence $\{s_k\}$ to obtain the MN-decimated sequences of

$$\begin{aligned}
V_0&=\{s_0, s_{MN}, s_{2MN}, \cdots\},\\
V_1&=\{s_1, s_{MN+1}, s_{2MN+1}, \cdots\},\\
&\cdots\cdots\cdots\cdots\\
V_{MN-1}&=\{s_{MN-1}, s_{2MN-1}, s_{3MN-1}, \cdots\},
\end{aligned}$$

then interleave each adjacent M of the MN-decimated sequences V_i's. Then, we obtain the (M, N) PSRG sequences T_i's in (4).

If a sequence S has the minimal MSRG expression $S_{MSRG}[G(x),\ D_0^g(x)]$ whose generating polynomial $G(x)$ is primitive of degree L and its period P is relatively prime to MN,[5] the 0th MN-decimated sequence V_0 has the minimal MSRG expression

$$V_0=S_{MSRG}[\hat{G}(x),\ \hat{D}_0^g(x)], \tag{5}$$

where $\hat{G}(x)$ is the primitive polynomial of degree L such that $\hat{G}(x)$ divides $x^{2^L-1}+1$ and $G(x)$ divides $\hat{G}(x^{MN})$, and the coefficient of x^j in $\hat{D}_0^g(x)$ is the coefficient of $x^{MN-1+jMN}$ in $D_0^g(x)\hat{G}(x^{MN})/G(x)$; and the 0th PSRG sequence T_0 has the minimal MSRG expression

$$T_0=S_{MSRG}[\overline{G}(x),\ \overline{D}_0^g(x)], \tag{6}$$

where $\overline{G}(x)=\hat{G}(x^M)$ and $\overline{D}_0^g(x)=\sum_{j=0}^{M-1} x^{M-1-j}\hat{D}_{jm}^g(x^M)$ for the smallest integer m meeting $mMN=1$ *mod ulo* P.[6]

For the minimal SSRG and MSRG for the 0th PSRG sequence T_0, the sequences generated by the $(ML-1-i)$th shift register of the SSRG and MSRG are denoted as U_i and W_i, $i=0, 1, \cdots, ML-1$, respectively, that is,

3. The notation $Q[G(x),\ x^L D_0^g(x)]$ denotes the quotient polynomial of $x^L D_0^g(x)$ divided by $G(x)$.
4. In this paper, summations and multiplications are all based on modulo-2 operations except for those in subscripts and superscripts.
5. The minimal MSRG for a sequence S is the smallest-lengthed MSRG whose MSRG sequence is identical to the sequence S.
6. Note that the jm the state polynomial $D_{jm}^g(x)$ can be obtained by taking the remainder polynomial of $x^{jm}\hat{D}_0^g(x)$ divided by $\hat{G}(x)$. Refer to [9] and [10].

$$U_i=\{d^c_{ML-1-i,k}\}, \tag{7a}$$

$$W_i=\{d^g_{ML-1-i,k}\}. \tag{7b}$$

Then, the ith PSRG sequence T_i, $i=0, 1, \cdots, N-1$, can be represented by

$$T_i=\sum_{j=0}^{L-1}\alpha_j^i U_{jM}, \tag{8a}$$

$$T_i=\sum_{j=0}^{L-1}\beta_j^i W_{jM}, \tag{8b}$$

where α_j^i and β_j^i, $i=0, 1, \cdots, N-1$, $j=0, 1, \cdots, L-1$, are such tnat[7]

$$R[\hat{G}(x), x^{iM+m}]=\sum_{j=0}^{L-1}\alpha_j^i x^j, \tag{9a}$$

$$Q[\hat{G}(x), x^L\sum_{j=0}^{L-1}\alpha_j^i x^j]=\sum_{j=0}^{L-1}\beta_j^i x^j. \tag{9b}$$

Ⅲ. Parallel Scrambling Techniques for DSS[8]

Since the scrambling and descrambling operations of the FSS are identical to those of the DSS, the parallel FSS techniques described in the previous section can also be applied to obtaining the PSRGs for the parallel DSS. But differently from the FSS, in the DSS the sampling of the scrambler SRG state and the correction of the descrambler SRG are needed for the synchronization of the scrambler and descrambler SRGs. Therefore, for the parallel DSS the sampling and correction circuits should be modified appropriately.

For this, we consider the *double sampling* and the *double correction* for the parallel DSS. The double sampling means that two samples are taken from the scrambler and the descrambler PSRG states at each sampling time, and the double correction means that two corrections of the descrambler PSRG state occur at each correction time. Note that in the case of length-L PSRGs J sets double sampling suffice to take all necessary PSRG samples, where J is $L/2$ when L is even and is $(L+1)/2$ when L is odd.

For a PSRG, the PSRG length L is the number of shift registers in the PSRG ; the *state vector* $\mathbf{d}_k$ (or $\hat{\mathbf{d}}_k$ in case the PSRG belongs to the descrambler) an L-vector representing the state of the shift registers in the PSRG at time k, that is,

$$\mathbf{d}_k \equiv [\, d_{0,k}\, d_{1,k} \cdots d_{L-1,k}\,]^t$$
$$(or\ \hat{\mathbf{d}}_k \equiv [\, \hat{d}_{0,k}\, \hat{d}_{1,k} \cdots \hat{d}_{L-1,k}\,]^t)\ ; \tag{10}$$

and the *state transition matrix* $\mathbf{T}$ an $L\times L$ matrix representing the relation between the state vectors $\mathbf{d}_k$ and $\mathbf{d}_{k-1}$, or more specifically,

$$\mathbf{d}_k=\mathbf{T}\cdot\mathbf{d}_{k-1}\ (or\ \hat{\mathbf{d}}_k=\mathbf{T}\cdot\hat{\mathbf{d}}_{k-1}). \tag{11}$$

For the sampling process, the ith *sampling time* is denoted as $r+i\alpha$, $i=0, 1, \cdots, J-1$, where r is a reference time and α is called *sampling interval*, and the *sampling vectors* for the two samples taken from the PRSG at each sampling time are denoted as $\mathbf{v}_0$ and $\mathbf{v}_1$ respectively.[9] Then, the two samples taken from the scrambler PSRG at the ith sampling time $r+i\alpha$ become $\mathbf{v}_0^t\cdot\mathbf{d}_{r+i\alpha}$ and $\mathbf{v}_1^t\cdot\mathbf{d}_{r+i\alpha}$ (or $\mathbf{v}_0^t\cdot\hat{\mathbf{d}}_{r+i\alpha}$ and $\mathbf{v}_1^t\cdot\hat{\mathbf{d}}_{r+i\alpha}$ for the descrambler PSRG). For the correction process, the ith *correction time* is denoted as $r+i\alpha+\beta$, $i=0, 1, \cdots, J-1$, where $\beta(0<\beta\leq\alpha)$ is called a *correction delay*, and the *correction vectors* for the two samples are denoted as by $\mathbf{c}_0$ and $\mathbf{c}_1$ respectively.[10] Then, the amount $(\mathbf{v}_0^t\cdot\mathbf{d}_{r+i\alpha}+\mathbf{v}_0^t\cdot\hat{\mathbf{d}}_{r+i\alpha})\,\mathbf{c}_0+(\mathbf{v}_1^t\cdot\mathbf{d}_{r+i\alpha}+\mathbf{v}_1^t\cdot\hat{\mathbf{d}}_{r+i\alpha})\,\mathbf{c}_1$ is added to the descrambler PSRG state vector

7. The notation $R[\hat{G}(x), x^{iM+m}]$ denotes the remainder polynomial of x^{iM+m} divided by $\hat{G}(x)$.
8. For a more detailed description on this, refer to [13].
9. The sampling vector for a sample is a vector representing the relation between the sampled value and the SRG state vector. A more detailed description on the sampling vector can be found in [6] or [7].
10. The correction vector for a sample is a vetor representing the positions of the shift registers in the descrambler SRG whose states are corrected. A more detailed description on the sampling vector can be found in [4] or [5].

$\hat{\mathbf{d}}_{r+i\alpha+\beta}$ at the ith correction time $r+i\alpha+\beta$ for the correction of the descrambler PSRG state. Fig.3 shows the sampling and correction diagram of the scrambler and descrambler PSRGs.

For a scrambler and descrambler PSRG pair, the *state error vector* δ_k is an L-vector representing difference between the scrambler PSRG state vector $\mathbf{d}_k$ and the descrambler PSRG state vector $\hat{\mathbf{d}}_k$, that is,

$$\delta_k \equiv \mathbf{d}_k + \hat{\mathbf{d}}_k. \tag{12}$$

Then the relation between the finally corrected state distance vector $\delta_{r+(J-1)\alpha+\beta}$ and the initial state distance vector δ_r becomes

$$\delta_{r+(J-1)\alpha+\beta} = \Lambda \cdot \delta_r, \tag{13}$$

where Λ is an $L\times L$ *correction matrix* which has the expression

$$\Lambda \equiv (\mathbf{T}^{\alpha} + \mathbf{c}_0 \cdot \mathbf{v}_0^t \cdot \mathbf{T}^{\alpha-\beta} + \mathbf{c}_1 \cdot \mathbf{v}_1^t \cdot \mathbf{T}^{\alpha-\beta})^{J-1} \cdot (\mathbf{T}^{\beta} + \mathbf{c}_0 \cdot \mathbf{v}_0^t + \mathbf{c}_1 \cdot \mathbf{v}_1^t). \tag{14}$$

Therefore, in order to achieve the synchronization the final state distance vector $\delta_{r+(J-1)\alpha+\beta}$ should be a zero vector regardless of the initial state distance vector δ_r, which can be done by making the correction Λ a zero matrix.

According to the *double sampling condition*, in order to make the correction matrix Λ in (14) a zero matrix for an appropriate β, $\mathbf{c}_0$ and $\mathbf{c}_1$, the sampling interval α and the sampling vectors $\mathbf{v}_0$ and $\mathbf{v}_1$ should be chosen such that the *discrimination matrix* Δ defined by

$$\Delta \equiv \begin{bmatrix} \mathbf{v}_0^t \\ \mathbf{v}_1^t \\ \cdots \\ \mathbf{v}_0^t \cdot \mathbf{T}^{(J-1)\alpha} \\ \mathbf{v}_1^t \cdot \mathbf{T}^{(J-1)\alpha} \end{bmatrix} \tag{15}$$

is of rank L. Note that the discrimination matrix Δ in (15) is a $2J\times L$ matrix, that is, $L\times L$ for an even L and $(L+1)\times L$ for an odd L.

The *double correction condition* shows how to choose a correction delay β and the correction vectors $\mathbf{c}_0$ and $\mathbf{c}_1$ making the correction matrix Λ a zero matrix, assuming that α, $\mathbf{v}_0$ and $\mathbf{v}_1$ satisfies the double sampling condition. According to the correction condition, for an even L the correction

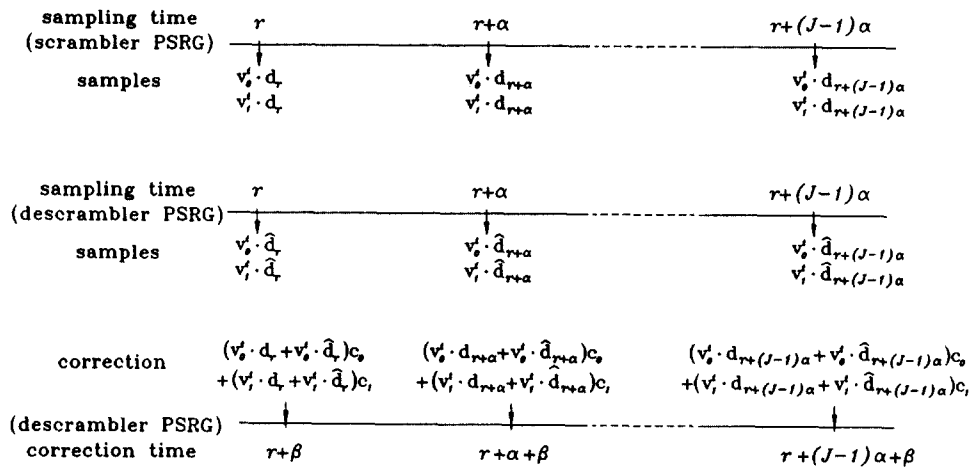

Fig. 3. The double sampling and double correction of the scrambler and descrambler PSRGs.

vectors $\mathbf{c}_0$ and $\mathbf{c}_1$ should have, for an arbitrary correction delay β, the expression

$$\begin{cases} \mathbf{c}_0 = \mathbf{T}^{(J-1)\alpha+\beta} \cdot \Delta^{-1} \cdot \mathbf{e}_{L-2}, \\ \mathbf{c}_1 = \mathbf{T}^{(J-1)\alpha+\beta} \cdot \Delta^{-1} \cdot \mathbf{e}_{L-1}, \end{cases} \tag{16}$$

where the L-vector $\mathbf{e}_i$, $i=0, 1, \cdots, L-1$, is the basis vector whose ith element is 1 and the others are 0.

For the case of an odd L, since the discrimination matrix Δ in (15) becomes an $(L+1)\times L$ matrix, the discrimination matrix Δ can be modified into the following two $L\times L$ matrices Δ_0 and Δ_1 :

$$\Delta_0 \equiv \begin{bmatrix} \mathbf{v}_1^t \\ \mathbf{v}_0^t \cdot \mathbf{T}^{\alpha} \\ \cdots \\ \mathbf{v}_0^t \cdot \mathbf{T}^{(J-1)\alpha} \\ \mathbf{v}_1^t \cdot \mathbf{T}^{(J-1)\alpha} \end{bmatrix}, \tag{17a}$$

$$\Delta_1 \equiv \begin{bmatrix} \mathbf{v}_0^t \\ \mathbf{v}_1^t \cdot \mathbf{T}^{\alpha} \\ \cdots \\ \mathbf{v}_1^t \cdot \mathbf{T}^{(J-1)\alpha} \\ \mathbf{v}_0^t \cdot \mathbf{T}^{(J-1)\alpha} \end{bmatrix}. \tag{17b}$$

Then, at least one of the two matrices Δ_0 or Δ_1 is nonsingular, in case the rank of the discrimination matrix Δ in (15) is L. If Δ_0 is nonsingular, the correction vector $\mathbf{c}_0$ and $\mathbf{c}_1$ should have, for an arbitrary correction delay β, the expressions

$$\begin{cases} \mathbf{c}_0 = \mathbf{T}^{(J-1)\alpha+\beta} \cdot \Delta_0^{-1} \cdot \mathbf{e}_{L-2} + u(\mathbf{v}_0^t \cdot \Delta_0^{-1} \cdot \mathbf{e}_{L-2}) \mathbf{T}^{(J-1)\alpha+\beta} \cdot \Delta_0^{-1} \cdot \mathbf{e}_0, \\ \mathbf{c}_1 = \mathbf{T}^{(J-1)\alpha+\beta} \cdot \Delta_0^{-1} \cdot \mathbf{e}_{L-1} + u(\mathbf{v}_0^t \cdot \Delta_0^{-1} \cdot \mathbf{e}_{L-1}) \mathbf{T}^{(J-1)\alpha+\beta} \cdot \Delta_0^{-1} \cdot \mathbf{e}_0, \end{cases} \tag{18}$$

where u is either 0 or 1.

Ⅳ. Parallel Scrambling for SDH Transmission

In this section, we consider parallel scramblers applicable to the SDH transmission systems employing the parallel scrambling techniques in the previous sections.

In the SDH transmission system, N of AUG(administrative unit group) signals are *byte-interleaved* in the unit of eight bits to form an STM-N payload, and SOH(section overhead) data are added to it to complete an STM-N signal. The frame format for this is shown in Fig.4. The STM-N

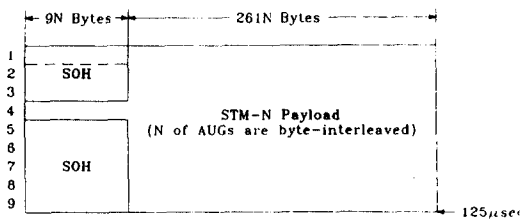

Fig. 4. Frame format for the STM-N signals.

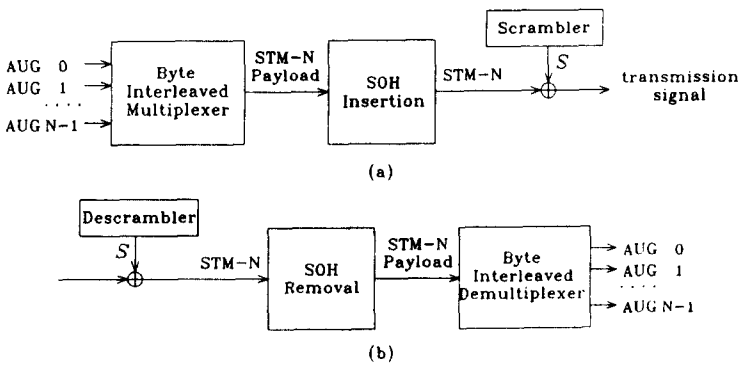

Fig. 5. Blockdiagram of the SDH systems.
(a)Transmitter, (b)receiver.

signal is scrambled, and then transmitted. The first $9N$ bytes of the frame(the shaded bytes in Fig.4) are excluded from the scrambling. In the receiver, the reverse operation of the transmitter is processed. The overall processing is depicted in Fig.5. The scrambler and descrambler are supposed to have the characteristic polynomial x^7+x^6+1 and to be reset to the state "1111111" at the beginning of each frame. This corresponds to the SSRG in Fig.6a with $C(x)=x^7+x^6+1$ and $D_0^c(x)=x^6+x^5+x^4+x^3+x^2+x+1$, which is equivalent, by (3a) and (3b), to the MSRG of Fig.6b with $G(x)=x^7+x+1$ and $D_0^g(x)=x^6+x^5+x^4+x^3+x^2+x$. In the figures, the numbers inside the shift registers represent the initial states. Since the first $9N$ bytes of the STM-N signal is excluded from the scrambling process, the scrambler and descrambler SSRGs(or MSRGs) resume the initial state $D_0^c(x)$(or $D_0^g(x)$) at the $(9N+1)$th byte of every frame.

The SSRGs(or MSRGs) we employ for the scrambler and descrambler of the SDH system operate at the speed of the STM-N signal rate, which is 155.520 Mbps for $N=1$, 622.080 Mbps for $N=4$, and 2.488320 Gbps for $N=16$. If we employ PSRGs instead of the SSRG(or MSRG) for the cases $N=4$ or 16, then the operating speed could drop from the STM-N rate to the STM-1 rate. This implies that the 622.080 Mbps or 2.488320 Gbps rate scrambling operation could be done at the 155.520 Mbps rate.

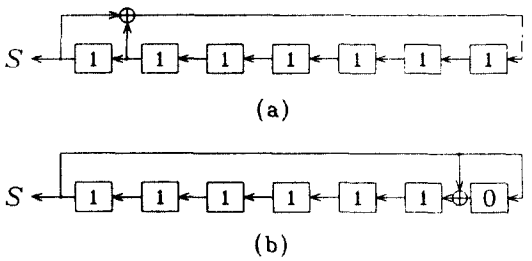

Fig. 6. The SRGs employed in the SDH systems.
(a)SSRG configuration, (b)MSRG configuration.

The SDH transmission system, when employing the parallel scrambling, is rearranged as shown in Fig.7. We observe from the figure that parallel scrambling is now performed prior to byte-interleaved multiplexer. The SOH insertion process should be modified accordingly. For the parallel scr-

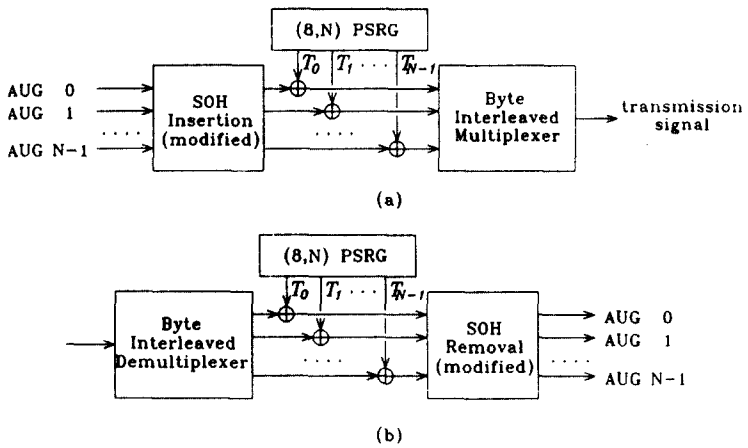

Fig. 7. Blockdiagram of the SDH systems employing byte-parallel scrambler.
(a)Transmitter, (b)receiver.

ambling we adopt an (8, N) PSRG since byte-interleaving is an 8-bit based operation. Note that what we should achieve in employing the parallel scrambling is to keep the transmission signal unchanged.

In the case of parallel scrambling of STM-4 signal, we need an (8,4) PSRG for the MSRG sequence $S_{MSRG}[x^7+x+1, x^6+x^5+x^4+x^3+x^2+x]$ of Fig.6b, whose generating polynomial $G(x)=x^7+x+1$ is primitive and its period $P=127$ is relatively prime to $MN=32$. By (5), the 0th 32-decimated sequence has the minimal MSRG expression

$$V_0=S_{MSRG}[x^7+x+1, x^6+x^5+x^3+x^2+x+1];$$

and by (6), the 0th PSRG sequence has the minimal MSRG expression

$$\begin{aligned}T_0=S_{MSRG}[&x^{56}+x^8+1, x^{55}+x^{54}+x^{53}+x^{52}+x^{51}+\\&x^{50}+x^{49}+x^{47}+x^{46}+x^{45}+x^{42}+x^{36}+x^{35}+x^{34}+\\&x^{31}+x^{27}+x^{26}+x^{24}+x^{23}+x^{22}+x^{21}+x^{20}+x^{19}+\\&x^{18}+x^{15}+x^{14}+x^{11}+x^7+x^6+x^2+x],\end{aligned}\quad (19a)$$

which can be, by (3a) and (3b), represented by the minimal SSRG expression

$$\begin{aligned}T_0=S_{SSRG}[&x^{56}+x^{48}+1, x^{55}+x^{54}+x^{53}+x^{52}+x^{51}+\\&x^{50}+x^{49}+x^{47}+x^{46}+x^{45}+x^{42}+x^{36}+x^{35}+x^{34}+\\&x^{31}+x^{27}+x^{26}+x^{24}+x^{23}+x^{22}+x^{21}+x^{20}+x^{19}+\\&x^{18}+x^{15}+x^{14}+x^{11}+x^5+x^4+x^3].\end{aligned}\quad (19b)$$

On the other hand, by (8a) and (9a), the PSRG sequences can be decomposed as

$$\begin{cases}T_0=U_0,\\ T_1=U_8+U_{16}=U_{32},\\ T_2=U_8+U_{32},\\ T_3=U_8+U_{24}+U_{48},\end{cases}\quad (20a)$$

and also by (8b) and (9b),

$$\begin{cases}T_0=W_0,\\ T_1=W_8+W_{16}=W_{32},\\ T_2=W_8+W_{32},\\ T_3=W_0+W_8+W_{24}+W_{48}.\end{cases}\quad (20b)$$

Therefore, noting that U_i, $i=0, 1, \cdots, ML-1$, is the $(ML-1-i)$th shift register output sequence of the minimal SSRG for T_0, we can depict, by (19b) and (20a), the SSRG-based (8,4) PSRG as shown in Fig.8a, and in a similar manner we can obtain, by (19a) and (20b), the MSRG-based (8,4) PSRG of Fig.8b.

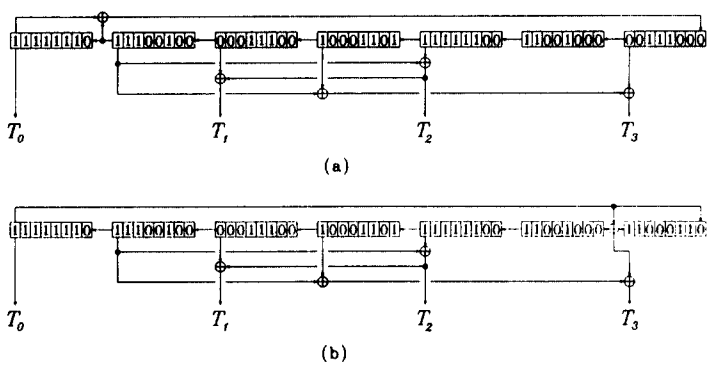

Fig. 8. An example of (8,4) PSRGs for parallel scrambling of the SDH signal STM-4.
(a)SSRG configuration, (b)MSRG configuration.

In the case of STM-16 signal, (8,16) PSRG configurations can be obtained in a similar manner to the case of the (8.4) PSRGs.

V. Parallel Scrambling for ATM Transmission

In this section, we consider parallel scramblers applicable to the ATM transmission systems. In the ATM transmission, there are two ways of transmitting ATM cells - the SDH-based and the cell-based transmissions. For the SDH-based transmission the FSS is applied to the STM frame, while for the cell-based transmission the DSS is used on the ATM cell stream.

In the SDH-based ATM transmission, ATM cells are mapped into the STM-1 or STM-4 signal, whose frame format is already shown in Fig.4, and then the STM signal is frame-synchronously scrambled using the SRG of Fig.6 in the same way as the SDH transmission described in Section Ⅳ. However, differently from the case of the SDH transmission, in the SDH-based ATM transmission there does not exist any multiplexing process. Therefore, in order to consider a parallel scrambling, we take the STM-1, or STM-4 signal as the M-bit multiplexed signal of the N lower-rate signals. Among various choices of M and N, we choose 1 for M and 8 for N, since it also matches the byte-level parallel processing. With this choice, we can expect the scrambling rates of 19.44 Mbps(=155.520/8) for the STM-1 signal and of 77.76 Mbps(=622.080/8) for STM-4 signal.

For this parallel scrambling, we need (1,8) PSRGs since M and N are 1 and 8 respectively, which can be obtained in the same manner as illustrated in Section Ⅳ. The resulting PSRGs are shown in Fig.9a and 9b.

In the cell-based ATM transmission, ATM cell stream is directly scrambled using the DSS which employs the SRG of the characteristic polynomial $C(x)=x^{31}+x^{28}+1$, as shown in Fig.10. The two uniformly distributed samples s_{t-211} and s_{t+1} of the SRG sequence $\{s_k\}$ are taken and conveyed over

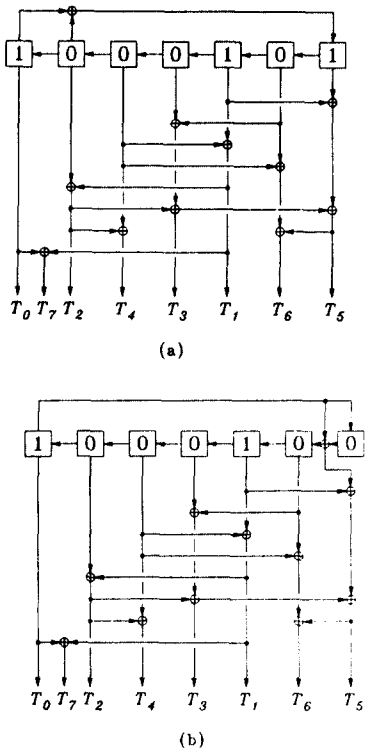

Fig. 9. An example of (1,8) PSRGs for parallel scrambling of the SDH-based ATM signals STM-1 and STM-4.
(a)SSRG configuration,
(b)MSRG configuration.

two contiguous bit slots in the HEC(Header Error Control) field of ATM cell as shown in Fig.11. The ATM cell size is 53 bytes (or 424 bits) and the transmission rate of ATM cell stream is 155.520 Mbps or 622.080 Mbps, which is the same as the SDH-based ATM transmission rate.

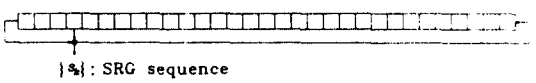

Fig. 10. The SRG employed for the DSS of the cell-based ATM transmission.

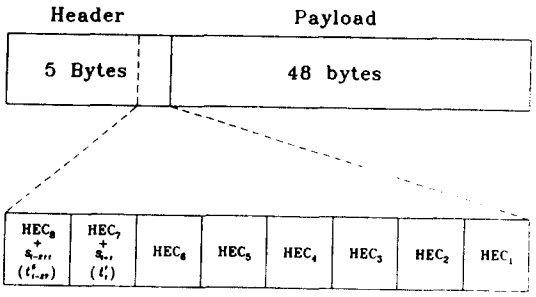

Fig. 11. Data structure for the DSS sample conveyance within ATM cell.

For the parallel scrambling of the ATM cell stream, we also take it as the (1-)bit interleaved multiplexed signal of the 8 lower-rate signals in the same way as the SDH-based ATM transmission. Then, we can also expect the scrambling rates of 19.44 Mbps and 77.76 Mbps for the two cell-based ATM transmission as in the case of the SDH-based ATM transmission.

Since the scrambling operation of the DSS is no different from that of the FSS, we can obtain an (1,8) PSRG in the same way as shown in Section Ⅳ. The resulting SSRG-based PSRG can be depicted in Fig.12. In this case, the length L is 31, and the state transition matrix $\mathbf{T}$ is

$$\mathbf{T}=[t_{i,j}]_{31\times 31},\ t_{i,j}=\begin{cases}1,\ j=i+1,\ i=0,\ 1,\ \cdots,\ 29,\\ 1,\ j=0\ \textit{or}\ 3,\ i=30,\\ 0,\ \textit{otherwise.}\end{cases}\qquad(21)$$

Noting that the bit-interleaved sequence of the eight parallel sequences $\{t^j_k\}$, $j=0,\ 1,\ \cdots,\ 7$, is identical to the serial SRG sequence $\{s_k\}$, we can find that the samples s_{t-211} and s_{t+1} of the scrambler SRG in the serial DSS correspond respectively to the samples t^5_{t-27} and t^1_t of the scrambler PSRG in the parallel DSS. Therefore, the sampling vectors $\mathbf{v}_0$ and $\mathbf{v}_1$ become

$$\mathbf{v}_0=[0100001000000000000010000000000]^t,\qquad(22a)$$

$$\mathbf{v}_1=[0010100000000000100000000000000]^t.\qquad(22b)$$

However the samples t^5_{t-27} and t^1_t are 27 (or 26) slots apart in parallel implementation, thus making it impossible to apply the double sampling scheme described in Section Ⅲ. So it is required to shift the sampling time of t^1_{t-27} to that of t^5_t for the application of the double sampling scheme.[11] By (11) we have the relation $t^5_{t-27}=\mathbf{v}_0^t\cdot\mathbf{d}_{t-27}=(\mathbf{v}_0^t\cdot\mathbf{T}^{-27})\cdot\mathbf{d}_t$, and hence the sampling vector $\hat{\mathbf{v}}_0$ for the sample t^5_{t-27} at the shifted sampling time t becomes

$$\hat{\mathbf{v}}_0=(\mathbf{T}^{-27})^t\cdot\mathbf{v}_0.\qquad(23)$$

Now that double sampling is possible, we have $\alpha=53(=424/8)$. Since $L=31$, we have $J=16$. Applying these numbers along with (21), (23) and

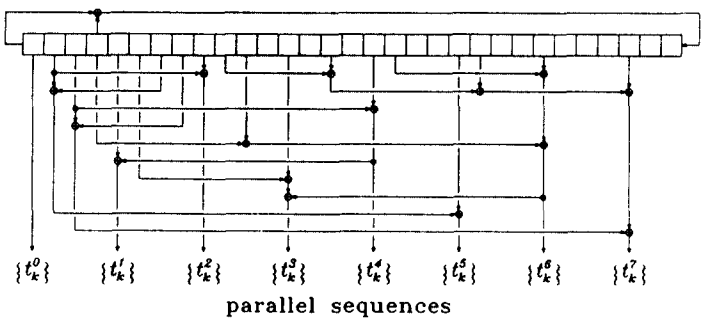

Fig. 12. A (1,8) PSRG for parallel scrambling of cell-based ATM signals.

11. A more detailed description on the sampling time shifting technique can be found in [7].

(22b) to (15) and (17), we can determine Δ, Δ_0 and Δ_1. Also, from the evaluated matrices, we confirm that Δ and Δ_0 are of rank 31.

For the double correction in the descrambler, we choose β, to be an in leger between 1 and α. Then, by (18) we obtain two sets of correction vectors c_0 and c_1. Note that the corresponding vectors vary depending on the choice of β, so the resulting circuit diagram of the descrambler also change accordingly.

Ⅵ. Conclusions

In this paper, we have investigated parallel scrambling techniques for use in today's two typical transmission systems – the SDH transmission system and the ATM transmission system. In the ATM transmission system, there are two ways of ATM cell transmission – the SDH-based and the cell-based transmission. For the SDH transmission and the SDH-based ATM transmission, the FSS is applied to the STM frames ; while for the cell-based ATM transmission, the DSS is used on the ATM cell stream.

We first briefly reviewed the parallel FSS and the parallel DSS techniques. In the case of FSS, the concept of PSRGs makes the parallel scrambling of FSS possible. The (M,N) PSRG is an SRG which generates N parallel sequences in such a way that when these sequences are M-bit interleaved the resulting sequence becomes identical to some prespecified sequence. To examine the properties of PSRGs, we considered the relation between the SSRG and the MSRG, and showed how to realize the PSRGs using the SSRG and the MSRG.

In the case of DSS, the double sampling and double correction play a main role in the parallel scrambling of DSS. The double sampling is a special sampling method which takes two samples from the scrambler and the descrambler PSRGs at each sampling time, and the double correction is also a special correction method which corrects the descrambler PSRG state two times at each correction time. For the double sampling, we considered the sampling time and sampling vector conditions, and for the double correction, we examined the correction time and correction vector conditions.

Based on these parallel scrambling techniques, we considered how to apply them to the SDH and the ATM transmissions. In the case of the SDH trasnsmission, N of AUG signals are byte-interleaved to form an STM-N payload, and the FSS is used on the STM-N frames. Therefore, setting $M=8$ to reflect the byte-interleaving, and setting $N=4$ to reflect the four base-rate signals within the STM-4, we could obtain an (8,4) PSRG which generates four parallel sequences for use in the corresponding parallel scrambler and descrambler. Repeating the parallelization by setting $N=16$, we can obtain an (8,16) PSRG for the STM-16.

In the case of the ATM transmission, differently from the SDH transmission, the data stream to be scrambled is originally serial. So we regarded the data streams of the SDH-based and the cell-based ATM transmission as the bit-interleaved multiplexed bitstreams of 8 base-rate signals, considering the byte-level parallel processing. For the SDH-based ATM transmission, since the same operation of FSS as the SDH transmission is applied to the STM frames, we could obtain an (1,8) PSRG for use in the corresponding parallel scrambler and descrambler. In the cell-based ATM transmission, the DSS is applied to ATM cell stream of the transmission rate 155.520 Mbps or 622.080 Mbps. In this case, the scrambler SRG samples are conveyed over the two contiguous time slots in each HEC field, and so the double sampling and correction is the most efficient in terms of circuit complexity.

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金 錫 昌(Seok Chang Kim) 正會員
1964年 8月 16日生
1987年 2月 : 서울大學校 電子工學科(學士)
1989年 2月 : 서울大學校 大學院 電子工學科(碩士)
1983年 3月 ~ 현재 : 同大學院 博士課程 在學

李 秉 基(Byeong Gi Lee) 正會員
1951年 5月 12日生
1974年 2月 : 서울大學校 電子工學科(學士)
1978年 2月 : 慶北大學校 電子工學科(碩士)
1982年 2月 : 美國 University of California, Los Angeles (Ph.D)
1982年 ~ 1984年 : 美國 Granger Associates 연구원
1984年 ~ 1986年 : 美國 AT&T Bell Laboratories 연구원
1986年 ~ 현재 : 서울大學校 電子工學科 副教授