Journal of Korean Association of Crystal Growth Vol. 4, No. 1 (1994) 42-45

Low temperature solution growth of silicon on foreign substrates

Soo Hong Lee and Martin A. Green*

Energy/Environment Lab., Materials & Device Research Center, Samsung Advanced Institute of Technology, Suwon 440-600, Korea *Center for Photovoltaic Devices and Systems, University of New South Wales, Kensington, N.S.W. 2033, Austrailia

이종기판을 사용한 저온에서의 실리콘 박막 용액 성장법

이수홍, Martin A. Green

삼성종합기술원 에너지환경연구실, 수원, 440-600

*Center for Photovoltaic Devices and Systems, University of New South Wales, Kensington, N.S.W. 2033, Austrailia

Abstract Deposition of silicon on pretreated sapphire and glass substrates has been investigated by the solution growth method at low temperatures. An average 14 μm thickness of silicon was grown over a large area on sapphire substrate originally coated with a much thinner silicon layer [0.5 μm (100) Si/(1 $\bar{1}$ 02) sapphire)] at low temperatures from 380 ~ 460 °C. Successful results were obtained from surface treated glass substrates in the temperature range from 420 ~ 520 °C.

요 약 금-비스무스 용매를 사용하여 실리콘 박막을 사파이어, 보로실리케이트 그라스 기판상에 성장시켰다. 사파이어의 경우 380~460℃에서 14 μm 두께의 실리콘막이 성장되었으며, 그라스 기판의 경우 420~520℃ 온도 범위에서 수백 μm 사이즈의 큰 결정립이 형성되었다. 이 결과는 저가의 박막태양전지를 제조하는데 응용될 것으로 사료된다.

1. Introduction

Many attempts have been made to prepare polycrystalline silicon thin film on foreign

substrates to obtain inexpensive solar cells [1,2] and thin film transistors [3]. Various substrates have been reported such as graphite, quartz, ceramic and glass. In particular there

has been an increasing interest in low temperature deposition of silicon on foreign substrates for use as solar cell [2,4]. Low temperature processing minimizes prospects for contamination from the substrate as well as reducing stress in the silicon thin film.

2. Solvent and growth apparatus

The solvent alloy was prepared from Au and Bi of 6N purity. The Si solubility in Au/Bi alloy is quite high at temperatures below 400°C in alloys containing up to 70 wt.% Bi. Solubilities in this and related solvents are summarized in other references [5,6]. A standard graphite slider boat approach [7] was used in this work. This boat, containing both a source wafer and the substrate, is placed in a furnace with a flowing nitrogen gas ambient. Prior to heating to the melt saturation temperature, the furnace was evacuated to 10^{-4} Torr (0.01 pascals) to remove oxygen and to test sealing integrity.

3. Substrate and its cleaning

The sapphire substrate was originally coated with a $0.5~\mu m$ thickness silicon layer which was grown by the conventional chemical vapour deposition (CVD) method. In this work, the original idea was to use this thin silicon layer as a seed to deposit a thicker layer (above $10~\mu m$) at much lower temperature. Glass is an extremely attractive layer onto which to deposit silicon thin film, due to its very effective role as the superstrate in present solar modules. In the current experiment, low expansion borosilicate glass (corning code 7740) was selected as the

substrate. The reasons are: these glasses are available commercially at relatively low cost and the thermal expansion coefficient of borosilicate glass is relatively well matched with silicon. To clean silicon on sapphire wafers, so called RCA 1 and RCA 2 solutions [8] were used for the silicon side, and boiling aqua regia solution (1 HNO₃ + 3 HCL) was employed for the sapphire side. A cold diluted mixture of 5% HF, 33% HNO₃, 2% Teefol and 60% H₂O was an effective solution for cleaning glass and silica [9]. Various cleaning methods for glass can be found in references [10].

Grown films on Si coated sapphire substrate

By using the standard sliding boat system, the growth of large area Si layers was demonstrated (Fig. 1). Due to the preferred nucleation of (100) oriented crystallites and the slower growth rate in the (111) direction, these films had a crystallographically influenced

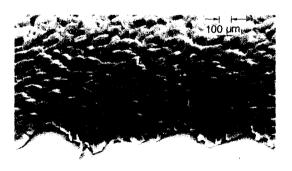


Fig. 1. SEM. The surface morphology of silicon layer on sapphire substrate (Sample ES-9, Growth temperature: $380 \sim 460$ °C).

rough surface texture. These rough films may be useful to trap light into cells fabricated upon them. This appears to be the first time that thick silicon has been deposited on sapphire substrate by the solution growth method at very low temperature. This experiment was a preliminary step before attempting silicon growth on glass substrate. For future work, depositing Si layers on uncoated sapphire substrate at lower temperature by using the solution growth technique is considered very valuable for novel device application.

5. Deposition on glass substrate

Si-coated glass substrate was prepared by initially sputtering 700 nm of silicon onto the glass, the surface of which had been roughened by sand blasting. Samples were furnace annealed at 820°C for 2 hours. After this annealing process, the samples were used as substrates for solution growth. The purpose of

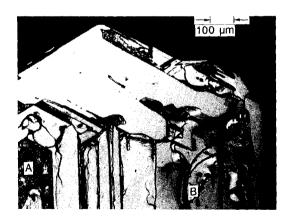


Fig. 2. The surface morphology of silicon layer on borosilicate glass substrate (Growth temperature: $420 \sim 550 \,^{\circ}\text{C}$).

the annealing process is to make fine grain polycrystalline silicon from the amorphous silicon prepared by sputtering.

The surface morphology of the silicon layer grown on silicon coated substrate is shown in Fig. 2. This morpology is similar to typical Si deposition on a (111) silicon substrate. The crystal shape has nearly hexagonal symmetry which shows the (111) preferred orientation. The (111) planes are the most closly packed in the silicon lattice. In general, the crystal planes that grow most slowly are those with the closest packing [11]. All the facets seem to be aligned. Some of the growth (A in Fig. 2) would occur after the slider moved because some remnant solvent melt still covered this area. The entire growth morphology appears to be consistent with terrace growth. This growth may be due to the roughened surface on the glass substrates. The semi-circular area (B in Fig. 2) was probably due to the presence of a depression or other impurities on the substrate which seem to be disturb the crystal growth front. No influence from the original silicon coating of the substrate could be observed. It might be concluded that the polycrystalline silicon, rather than acting as a seed, merely improved wettability between the melt and the substrate. Some factors that influence nucleation of silicon on glass substrates are discussed below. Firstly, supersaturation and high silicon content are important in encouraging nucleation on the glass. In the present work, the cooling rate was above 3°C/min. The silicon solubility in Au-60 wt. % Bi solvent is about 2.2 at.% at 414°C and 4.5 at.% at 513°C. Compared to Sn melt (2 at. % at 950° C), this alloy has a high content of silicon at much lower temperature. Secondly, surface treatments probably improved wettability between the melt and the substrate. Good wetting is a prerequisite for fabricating continuous layers.

6. Conclusion

Silicon deposition on sapphire and borosilicate substrates was investigated by the solution growth method at very low temperatures. An average 14 μ m silicon was grown over a large area on silicon coated sapphire substrate [(100) silicon on (1102) sapphire]. These films seem suitable for the fabrication of high efficiency silicon solar cells. Successful results were obtained from furnace annealed glass substrates coated with sputtered silicon. A continuous silicon thin film on a large area substrate was obtained in the temperature range from 420 ~ 520 °C. These films might be applied to lower the cost of solar cells.

Acknowledgements

This work was supported by the Australian National Energy Research. Development and Demonstration Program and the New South Wales Department of Minerals and Energy. The Centre for Photovoltaic Devices and System is supported by the Australian Research Council

Special Research Centres Scheme and Pacific Power.

References

- [1] T.L. Chu, J. Crystal Growth 39 (1977) 45.
- [2] J.B. McNeely, R.B. Hall, A.M. Barnett and W.A. Tiller, J. Crystal Growth 70 (1984) 420.
- [3] W. Czubatyj, D. Beglau, R. Himmler, G. Wicker, D. Jablonski and S. Guha, IEEE Electron Device Letters 10 (1989) 10.
- [4] B. Girault, F. Chevrier, A. Joullie and G. Bougnont, J. Crystal Growth 37 (1977) 169.
- [5] S.H. Lee, S.A. Healy, T.L. Young and M. A. Green, Materials Letter 9 (1990) 53.
- [6] S.H. Lee and M.A. Green, J. Electronic Materials 20 (1991) 635.
- [7] H. Nelson, US Patent 3, 565, 702 (1971).
- [8] W. Kern and D.A. Puotinen, RCA Review 31 (1970) 187.
- [9] R.H. Crawley, Chem. Ind. 45 (1953) 1205.
- [10] P.B. Adams, J. Testing and Evaluation 5 (1977) 53.
- [11] T.F. Ciszek, J. Electrochem. Soc. 132 (1985) 422.